ECED2200 – Lab #7

STUDENT NAME(s): _____ .

STUDENT NUMBER(s): B00 _____ .

Pre-Lab Information

It is recommended that you read this entire lab ahead of time. Doing so will save you considerable time during the lab.

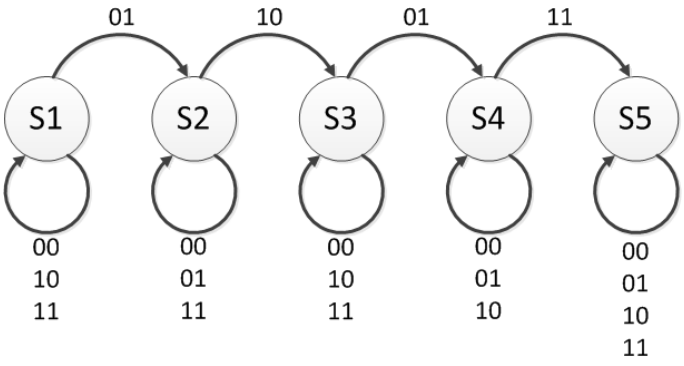
There is also several videos showing the use of the software tools – you will save considerable time by watching those now. See http://www.colinoflynn.com/teaching and look at the 'lab 7' information.

Overall Objective

In this lab you will use VHDL to write a simple state machine.

Design Specifications for State Machine

You are required to design a state machine which moves between five possible states. Once it reaches the final state it stays in that state until an external reset moves it back to the original state.



The above diagram shows for example that from state 1, we only move to state 2 when SW1=0 and SW2=1. Once we reach state 2 we stay in that state until SW1=1 and SW2=0. The required input to cause a transition for each additional state is shown.

Note: You may wish to see the video instructions for this lab, which show the state machine moving between each state.

The output for each state is simply to light an LED indicating the state number. In state S1 we light LED1, in state S2 we light LED2, etc. This is shown in the table below:

State	LED1	LED2	LED3	LED4	LED5
S1	1	0	0	0	0
S2	0	1	0	0	0
S3	0	0	1	0	0
S4	0	0	0	1	0
S5	0	0	0	0	1

Deliverables

You will work individually for this lab. Each person must deliver a lab report; the format for it is described separately.

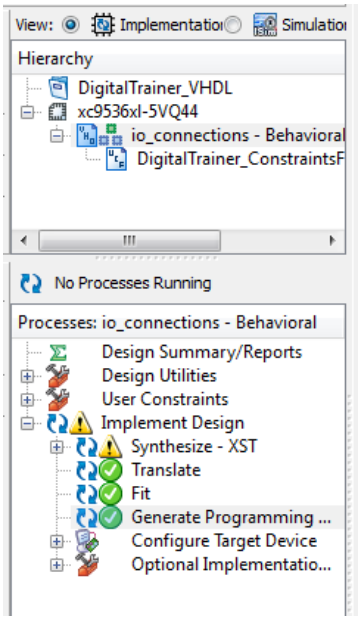
Required Materials

- Computer with Xilinx ISE 13.2 Webpack installed.
  - All computers in the lab have this installed.
  - This is free software so you can install on your own computer if you wish, you can download it from http://www.xilinx.com/support/download/index.htm - select '13.2' on the side. The file is very large so you may wish to download at school, and you are required to register to license it.
- Example project file DigitalTrainer_VHDL_lab7.zip
  - This file contains an environment which is already setup for your lab.
- Digital Trainer Board

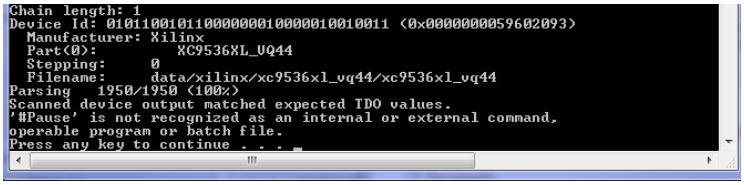
Procedure

1. Download DigitalTrainer_VHDL_lab7.zip from www.colinoflynn.com/teaching under the ECED2200 lab #7.
2. Unzip this somewhere.
3. Open the DigitalTrainer_Simple.xise
4. Open io_connections.vhd
5. Implement the remaining part of the state machine. This file is partially complete in that it shows the correct transition from state S1 to S2. You will need to add the logic to move through the rest of the states.

6. As before, double-click the 'Implement Design' process, and you should get green Check-marks besides 'Generate Programming File':



7. Plug in your Digital Explorer board.
8. Run 'program.bat' as before, and again you should see an indication it is successful:



9. Move the switches through the specified pattern from the design specifications; confirm it moves through each state as required. Note the input clock is 1 Hz, so the switches are only sampled every 1 second.

Observations

Include your VHDL source code. This is the 'io_connections.vhd' file.

Conclusion

In this lab you have learned about how to use VHDL for making a simple state machine.