ECED2200 – Lab #1

STUDENT NAME(s): _____ .

STUDENT NUMBER(s): B00 _____ .

Pre-Lab Information

It is recommended that you read this entire lab ahead of time. Doing so will save you considerable time during the lab.

You will be required to build an OR gate using only a single NAND chip, which contains four NAND gates. Using *four or less* NAND gates design a circuit that behaves as an OR gate. You can record this design in the 'observations' section of this lab.

There is also several videos showing the use of the software tools – you will save considerable time by watching those now. See http://colinoflynn.com/teaching/eced2200-intro-to-digital-circuits/ and look at the 'lab 1' information.

Overall Objective

This lab has three main objectives: using breadboards with physical chips, simulating designs with Xilinx ISE tools. This lab will thus be split into two parts.

Deliverables

There is no lab report required for this lab. Fill out the following during the lab, and hand this report in:

1. Your Name
2. The tables in the 'Observations' of each Part
3. The blank schematics & layout in the 'OR GATE Built from NAND Gate' of Part-1
4. The Questions at the end of the report

Part #1: Using Breadboards with Physical Chips

Objective

- Familiarize yourself with reading schematics of digital logic chips and translating them into physical designs
- Verifying the truth tables of several basic logic chips
- Construct an OR gate from a NAND-gate chip

- Identify a mystery chip

Required Materials

- Dalhousie Digital Trainer Board
- 7408 AND Gate
- 7432 OR Gate
- 7400 NAND Gate
- 7486 XOR Gate
- Mystery Chip

Background

Procedure

1. Plug your BORA board into your computer using a Mini-USB Cable

2. Download BORA_Eraser.zip from https://www.assembla.com/spaces/bora/documents/d7PlO8DZqr46bTacwqjQYw/download/d7PlO8DZqr46bTacwqjQYw (also referenced from colinoflynn.com/teaching)

3. Unzip the BORA_Eraser.zip somewhere, and double-click on 'erase_all.bat' to clear the BORA board. **This step is critical for the LEDs/Switches to work**. Once this is complete all LEDs should be slightly lit. Do not simply open the BORA_Eraser.zip folder & click erase.bat, you MUST COPY FILES OUT.

4. A schematic is given for each of the gates we investigate. Build each circuit on the Digital Trainer. Vary the inputs and observe the outputs to build up the truth table. If the connected LED is off the output is at logic 0, if the LED is on the output is at logic 1.

5. Design an OR gate using only a single NAND gate chip (that is the 7400 chip). Implement this design, record the design in the 'observations', and record the resulting input/output.

6. You will be given a 'mystery chip'. The mystery chip uses the same pinout as the 7400 chip, but is not necessary a NAND gate. Observe the truth table of the mystery chip and find the type of gate this chip has implemented. It may be any one of the following chips: AND, NAND, OR, NOR, XOR, XNOR. Each mystery chip is different, so your results will differ from other groups.

Observations

7408 AND Gate Truth Table:

A	B	Y
0	0	

0	1	
1	0	
1	1	

7432 OR Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

7400 NAND Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

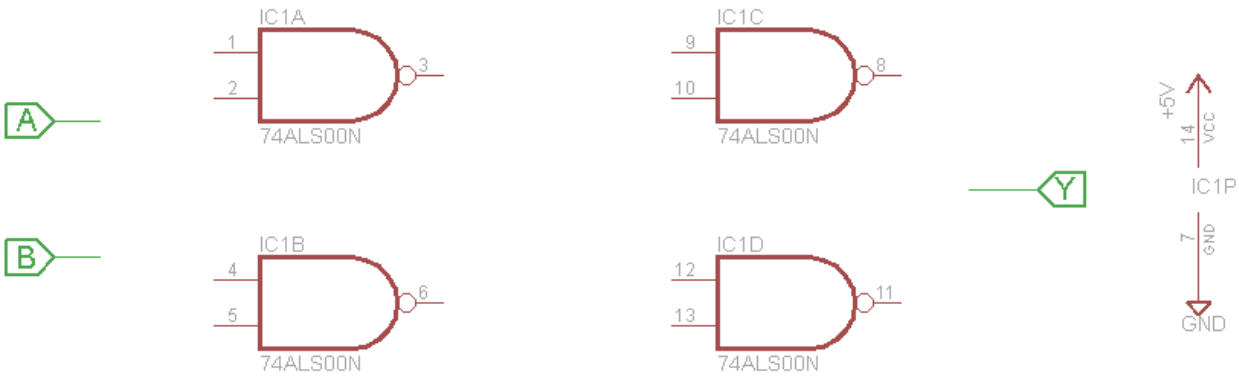
7486 XOR Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

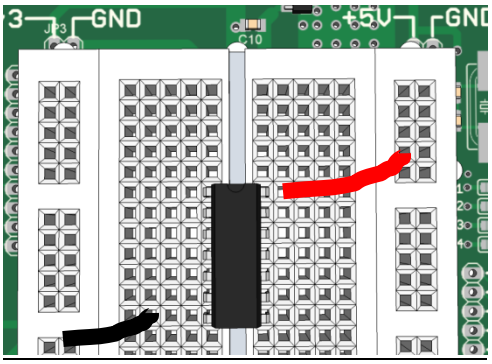
OR Gate Built from NAND Gates:

Schematic:

Digital Circuits – Lab #1



Implementation:



Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Mystery Chip:

A	B	Y
0	0	
0	1	
1	0	
1	1	

My Mystery Chip number is ____. Based on the truth table it is a(n) _____ gate.

Part #2: Simulating Designs with Xilinx ISE Tools

Objective

- Familiarize yourself with Xilinx ISE tools
- Learn about the use of 'schematic-entry' design
- Run a simple simulation with pre-defined stimulus

Required Materials

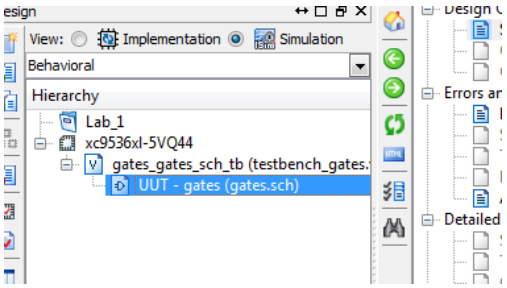
- Computer with Xilinx ISE 13.2 Webpack installed.
    - All computers in the lab have this installed.
    - This is free software so you can install on your own computer if you wish, you can download it from http://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/design-tools/v13_2.html The file is very large so you may wish to download at school, and you are required to register to license it (which is free).
- Example project file http://colinoflynn.com/teachingfiles/eced2200/lab1.zip
    - This file contains an environment which is already setup for your lab. If you have time you may wish to recreate this from scratch. There is a video available showing this linked from http://colinoflynn.com/teaching

Background

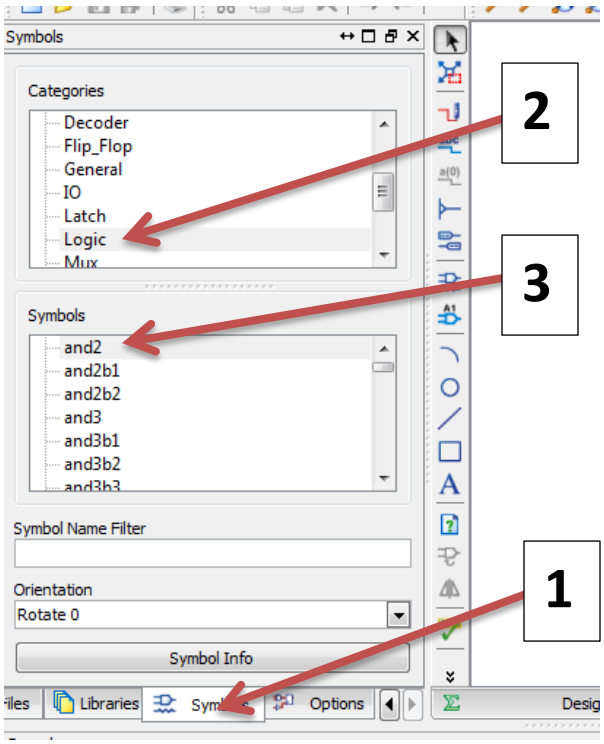
Procedure

NOTE: There is a video version of this procedure at http://colinoflynn.com/teaching which will be much easier to follow along with. If you have a smartphone/tablet it may also be useful to open the video on your portable device instead of the computer.

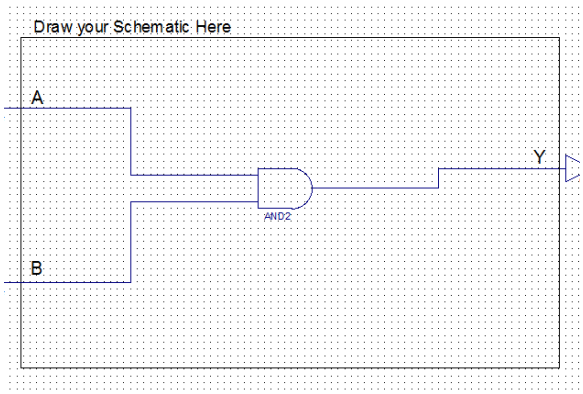
1. Unzip the ZIP file somewhere – **you MUST copy all the files out of the ZIP, do NOT just attempt to open the zip file & run from within that**.
2. Double-click on the file 'Lab_1.xise' which will open Xilinx ISE Project Navigator. This step may take a moment for the software to open.
3. Double-click on the 'UUT' schematic file:



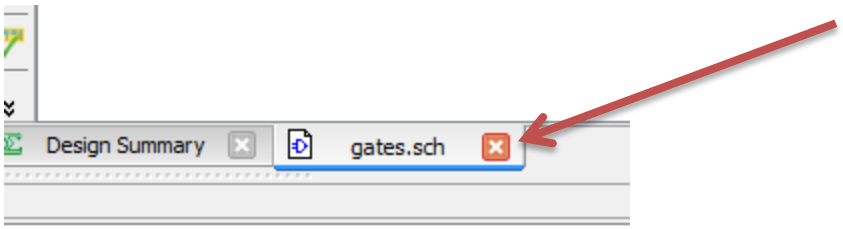
4. Go to the 'symbols' tab in the window that opens, select 'Logic' as the category, and 'and2' as the Symbol:



5. Place the AND gate into the area which says 'draw your schematic here'. You may need to zoom in, then connect up the inputs and outputs with the wire command:



6. Save the file, then close JUST that file (NOT the whole project):

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or to edit gates.sch".
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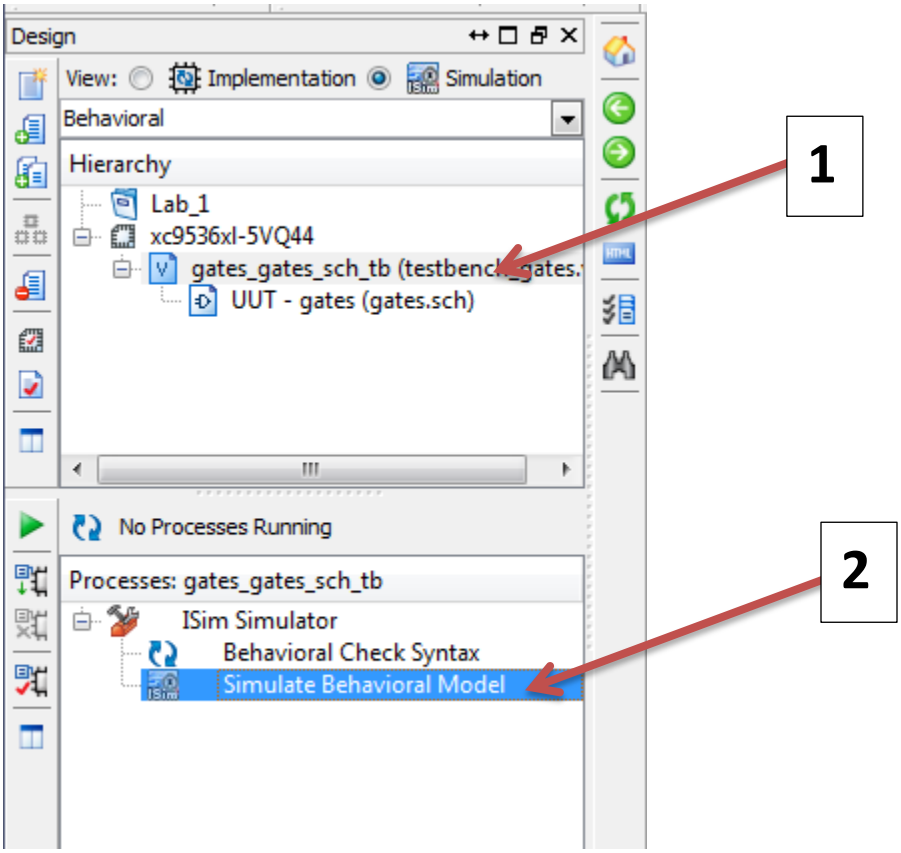
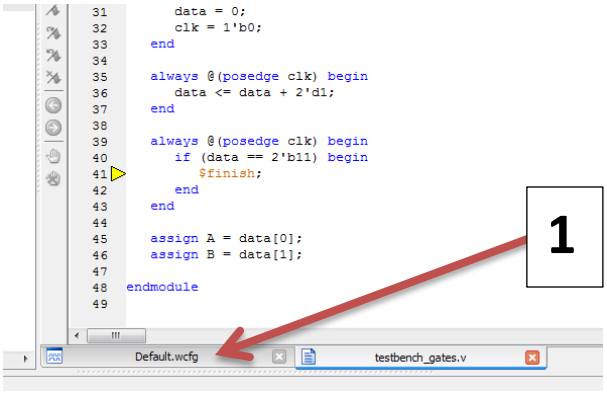
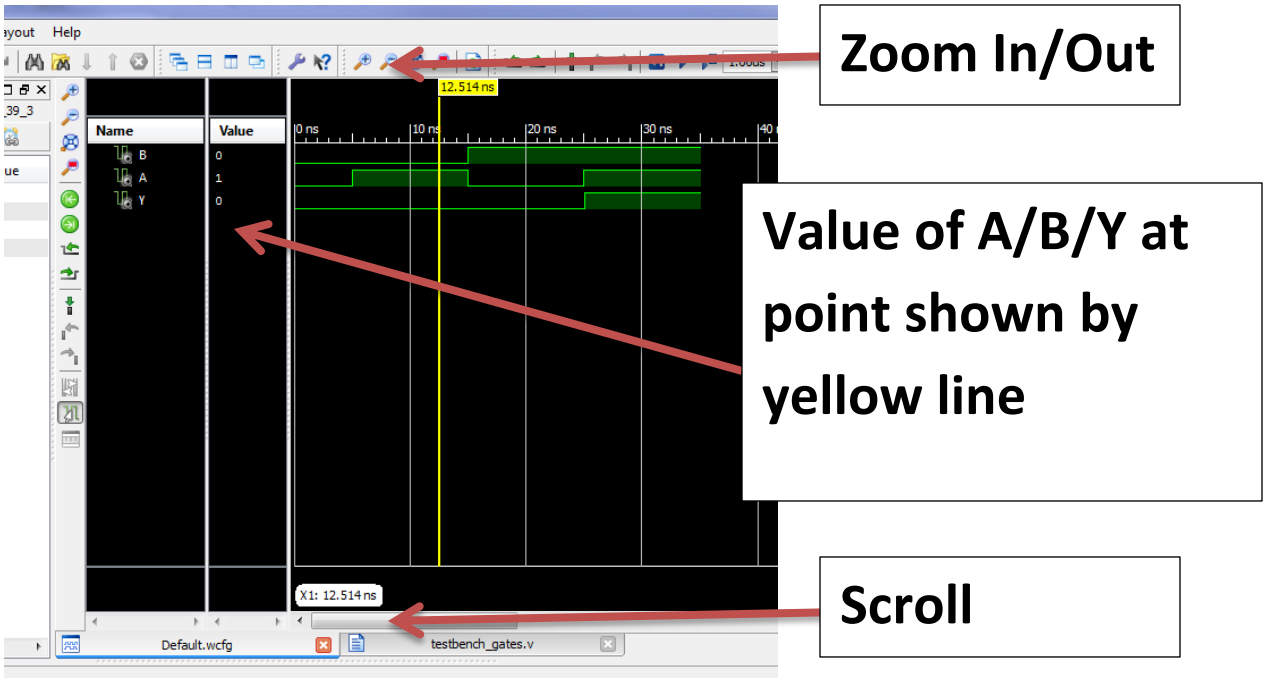
7. Select ‘gates_gates_sch_tb’, then double-click ‘Simulate Behavioural Model’. You may need to hit the ‘+’ beside ‘ISim Simulator’:



8. In the window that opens, change to the ‘Default.wcfg’ tab:



9. Using the waveform display, fill in the truth table. You may need to scroll the waveform to start at time 0 or zoom in/out. You can click on different times in the waveform and just read A/B/Y directly off. Fill in the observations based on this.



10. Close the ISim window, it will ask if you really want to exit the application, hit “Yes”.
11. Open the gates.sch file again and delete the AND gate.
12. Repeat steps 1-12 with the following gates:
    a. or2
    b. nand2
    c. xor2
    d. xnor2
    e. nor2b1

Observations

AND2 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

OR2 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

NAND2 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

XOR2 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

XNOR2 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

NOR2B1 Gate Truth Table:

A	B	Y
0	0	
0	1	
1	0	
1	1	

Conclusions

In this lab you've built a physical circuit on a digital trainer board, and then used the Xilinx ISE software to simulate a similar circuit. In future labs we'll learn how to use the Xilinx ISE software to actually download the design to the BORA board.