

ECED2200 – DIGITAL CIRCUITS

Programmable Logic

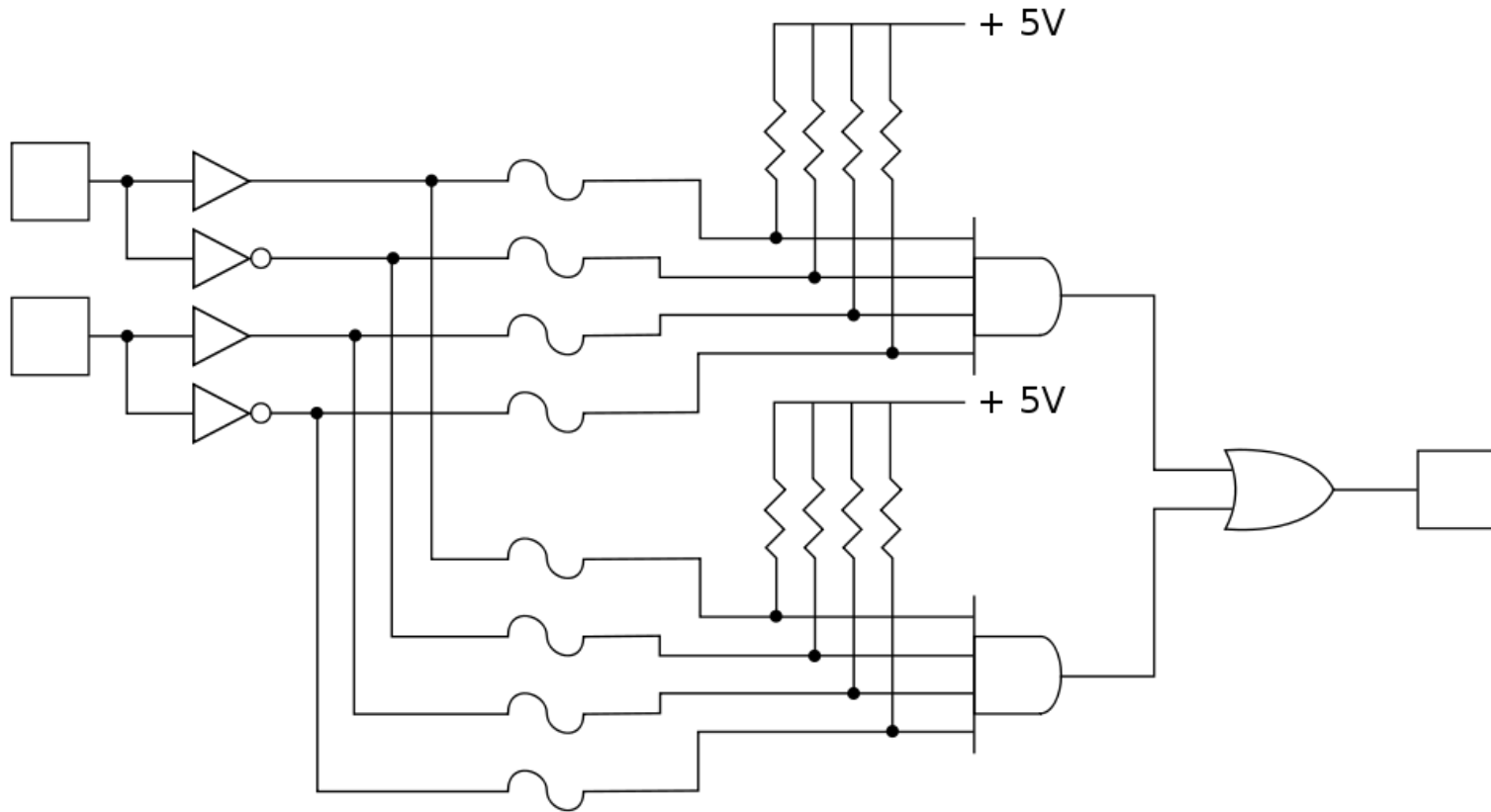
GENERAL NOTES

- See updates to these slides: www.newae.com/teaching
- These slides licensed under '[Creative Commons Attribution-ShareAlike 3.0 Unported License](http://creativecommons.org/licenses/by-sa/3.0/)'
- These slides are not the complete course – they are extended in-class
- You will find the following references useful, see www.newae.com/teaching for more information/links:
 - The book “Bebop to the Boolean Boogie” which is available to Dalhousie Students
 - Course notes (covers almost everything we will discuss in class)
 - Various websites such as e.g.: www.play-hookey.com
 - The book “Contemporary Logic Design”, which was used in previous iterations of the class and you may have already

IMPLEMENTING DESIGNS

		A B					
		0 0	0 1	1 1	1 0		
C	0	$\bar{A} \cdot \bar{B} \cdot \bar{C}$	$\bar{A} \cdot B \cdot \bar{C}$	$A \cdot B \cdot \bar{C}$	$A \cdot \bar{B} \cdot \bar{C}$		
	1	$\bar{A} \cdot \bar{B} \cdot C$	$\bar{A} \cdot B \cdot C$	$A \cdot B \cdot C$	$A \cdot \bar{B} \cdot C$		

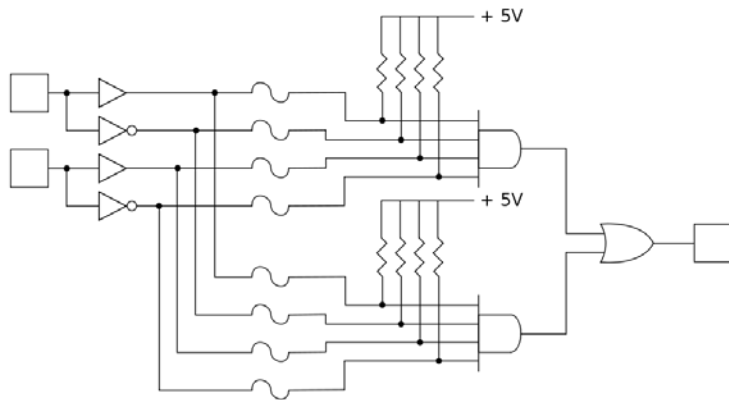
PROGRAMMABLE ARRAY LOGIC (PAL)



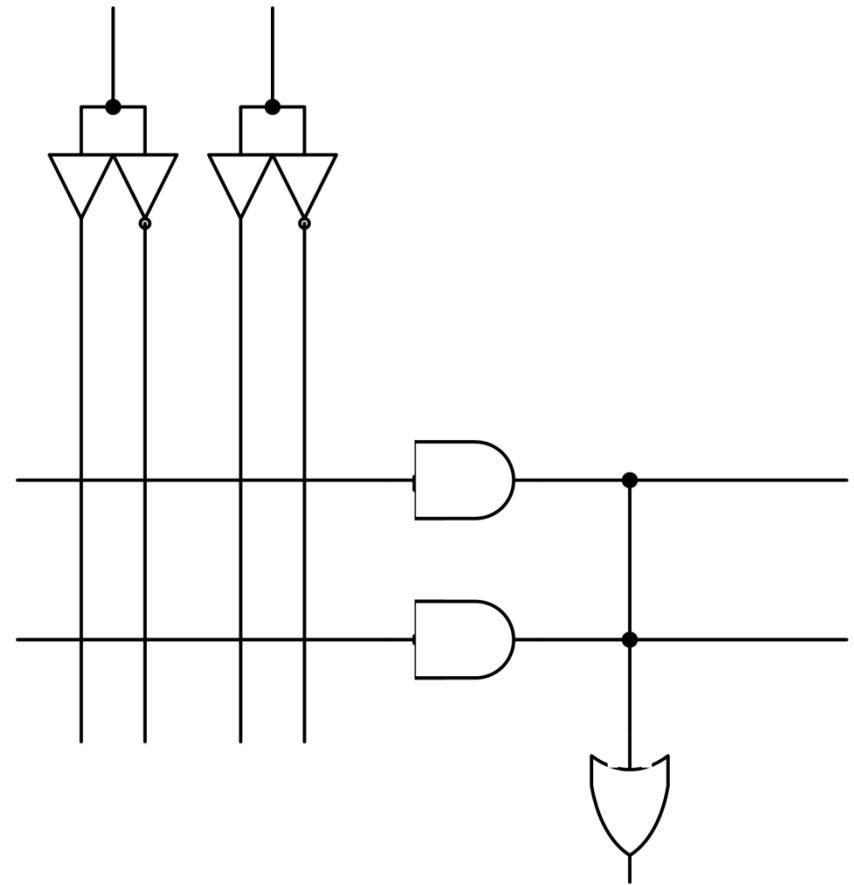
Simplified programmable logic device

Source: http://en.wikipedia.org/wiki/File:Programmable_Logic_Device.svg

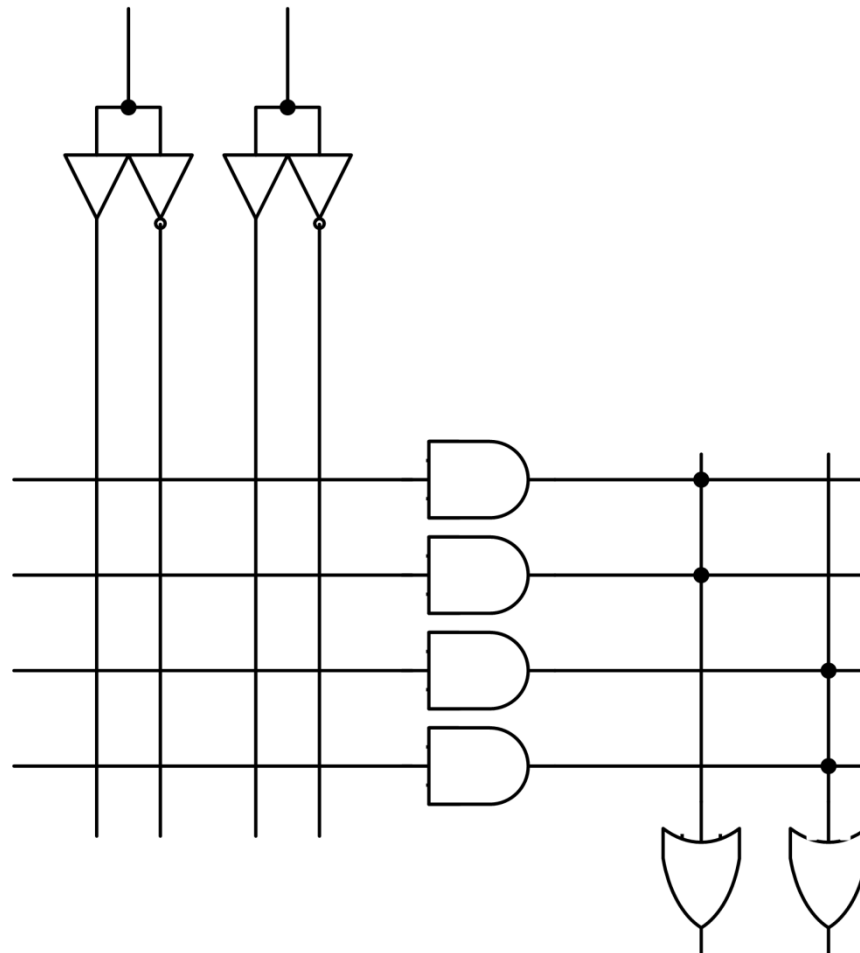
PROGRAMMABLE ARRAY LOGIC (PAL)

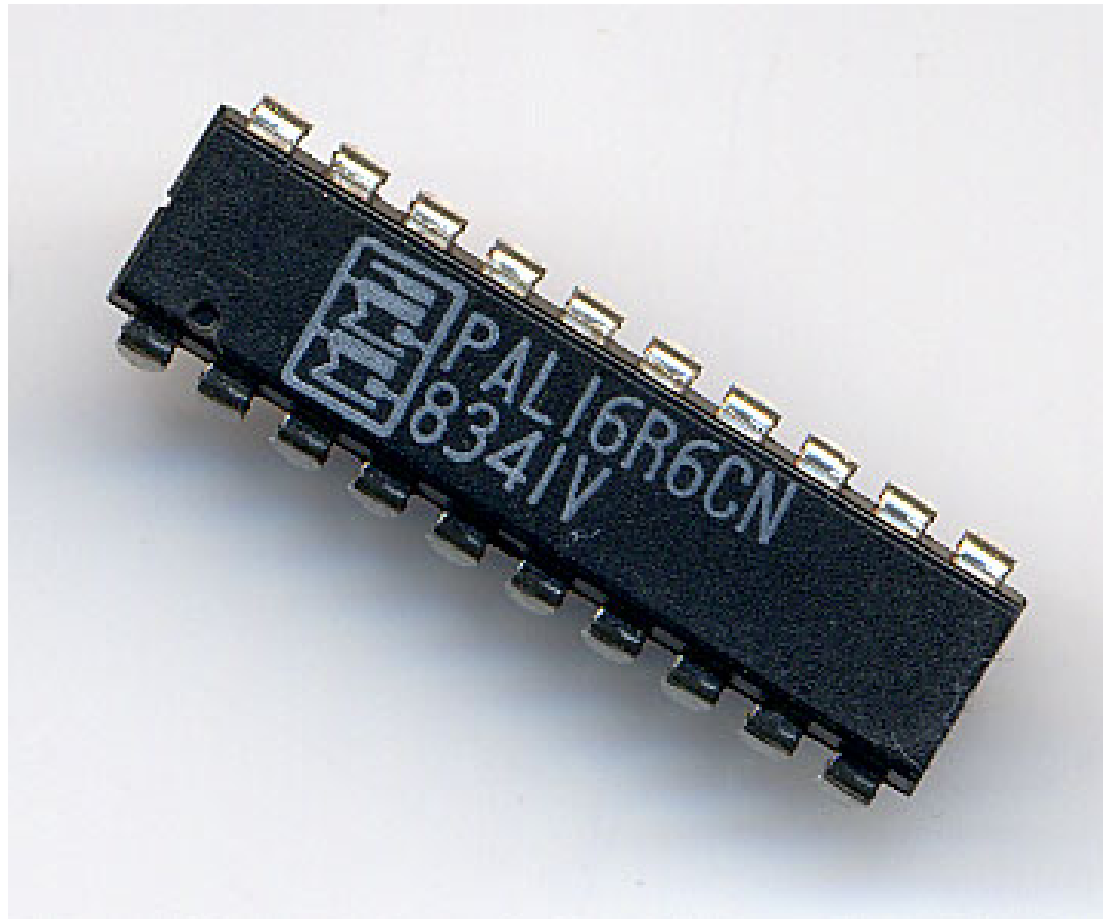


Simplified programmable logic device

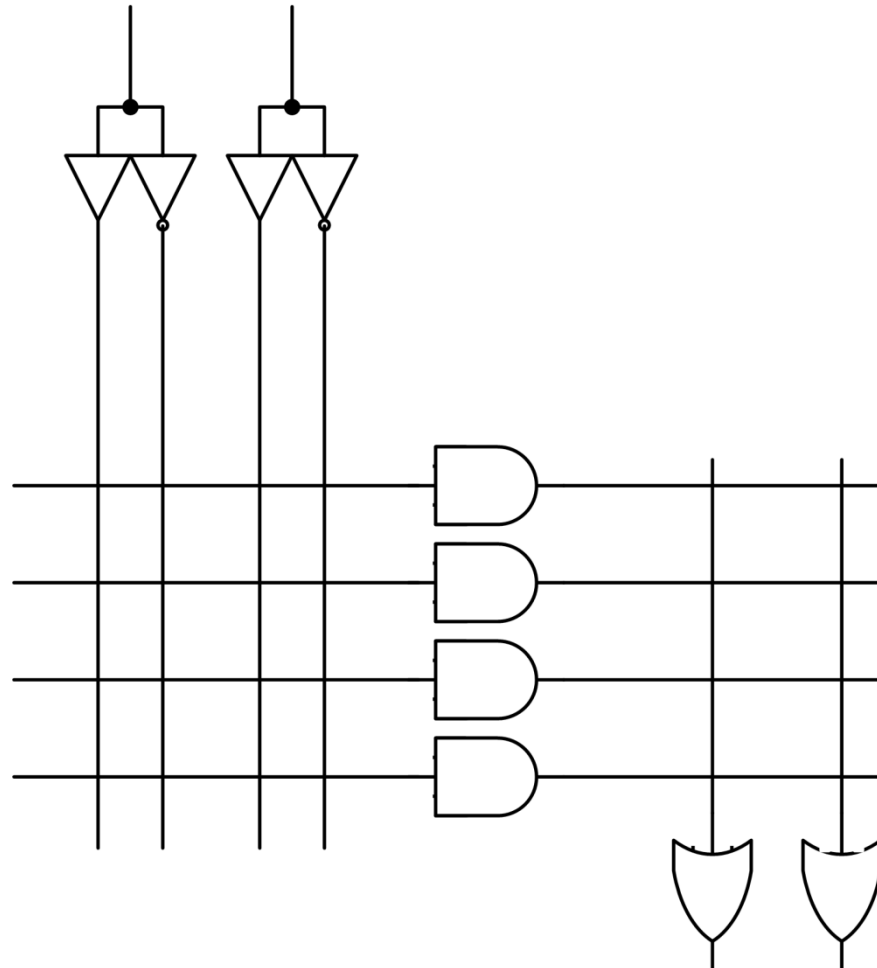


PROGRAMMABLE ARRAY LOGIC





PROGRAMMABLE LOGIC ARRAY (PLA)

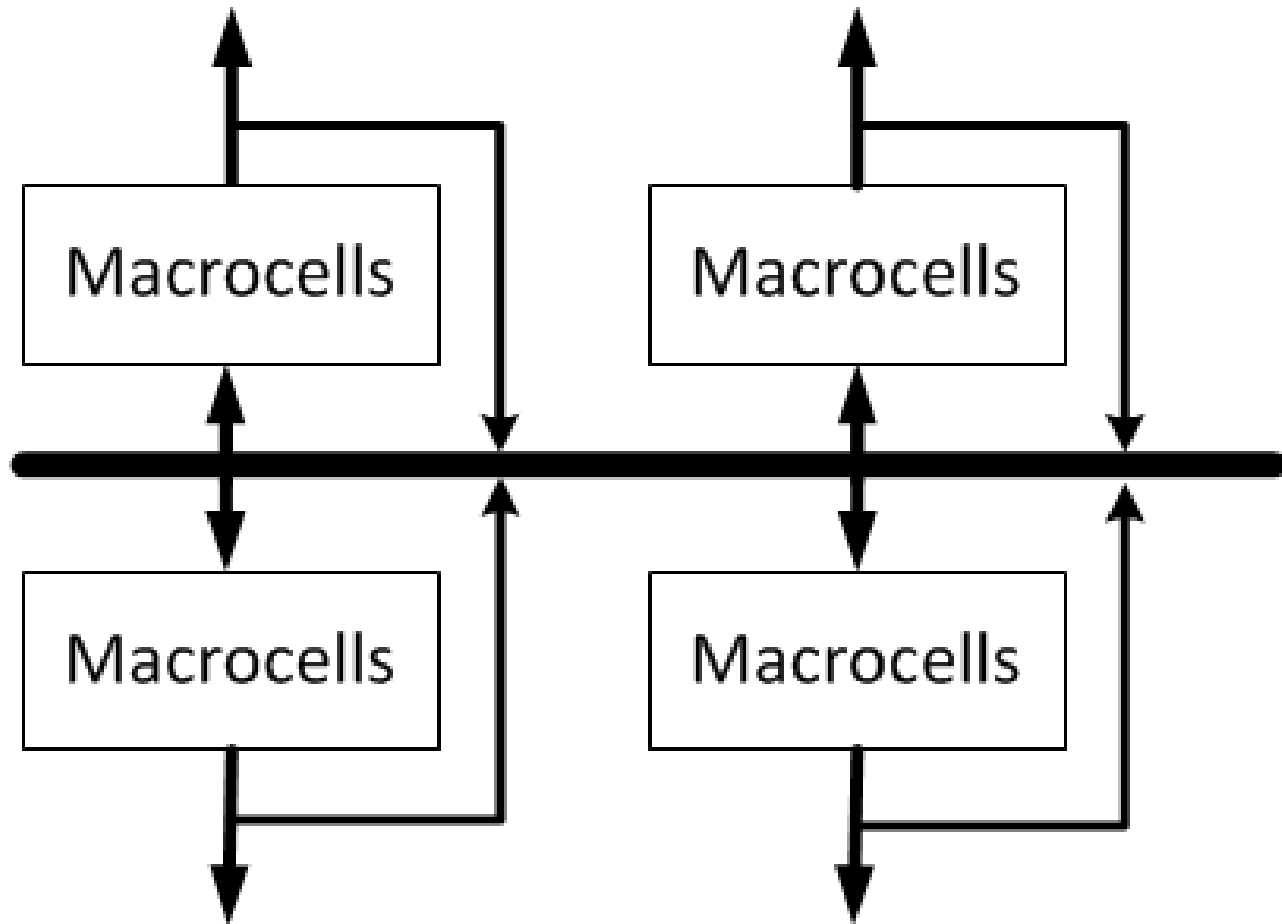


PAL vs PLA

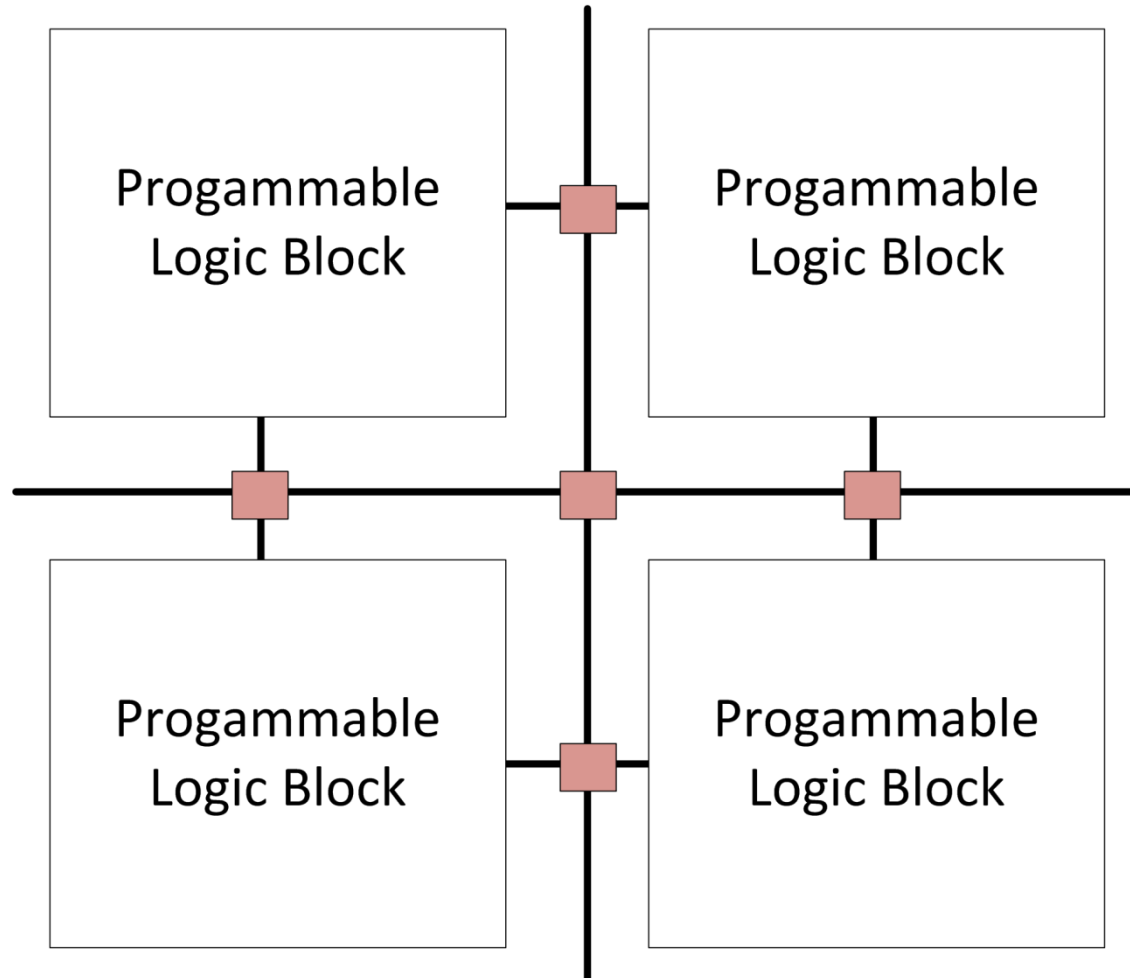
PAL = AND inputs fused, OR inputs fixed

PLA = AND inputs fused, OR inputs fused

COMPLEX PROGRAMMABLE LOGIC DEVICES



FIELD PROGRAMMABLE GATE ARRAYS



TIMELINE

1975: First PLAs become available

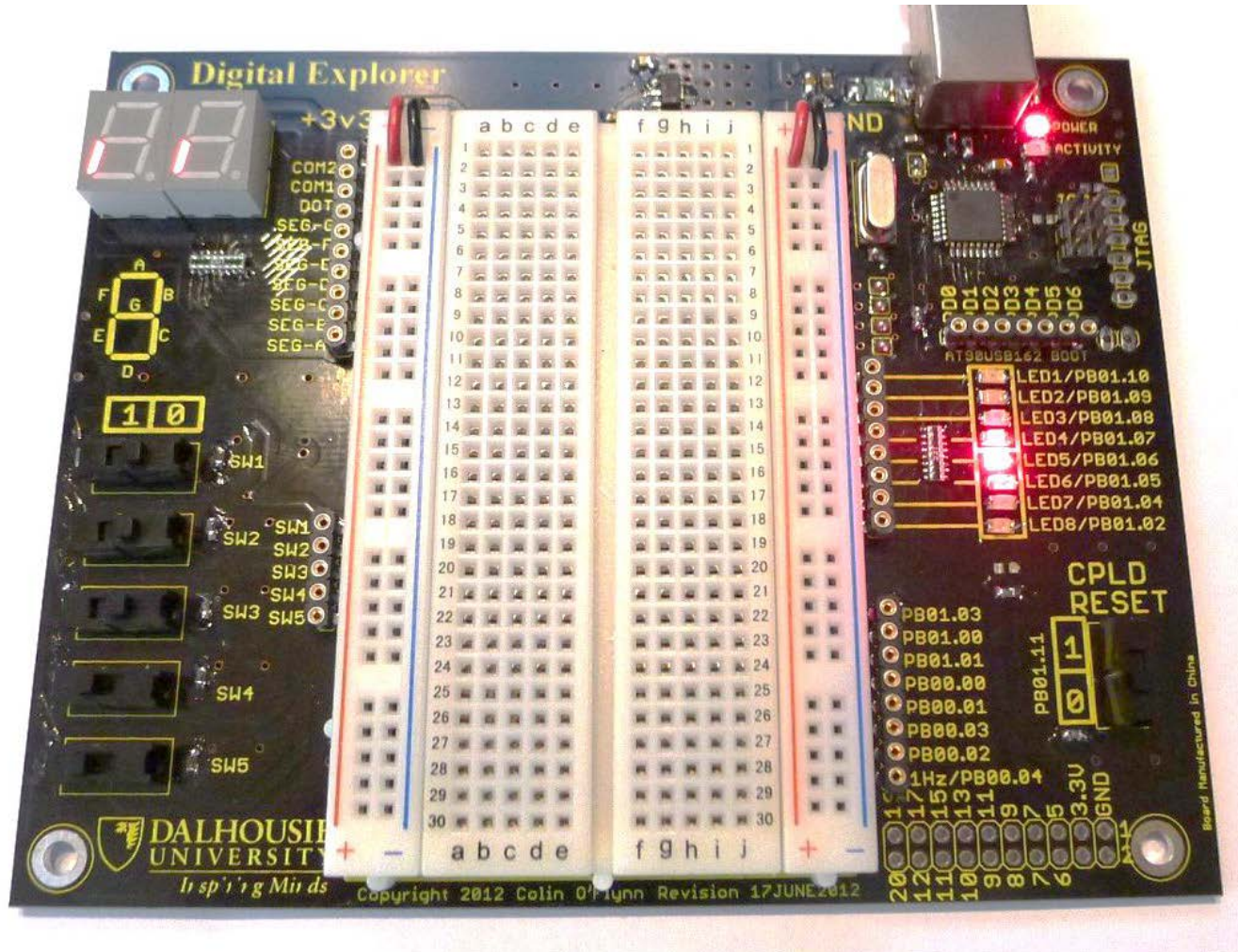
1978: First PAL (MMI)

1983: First GAL (Lattice Semi)

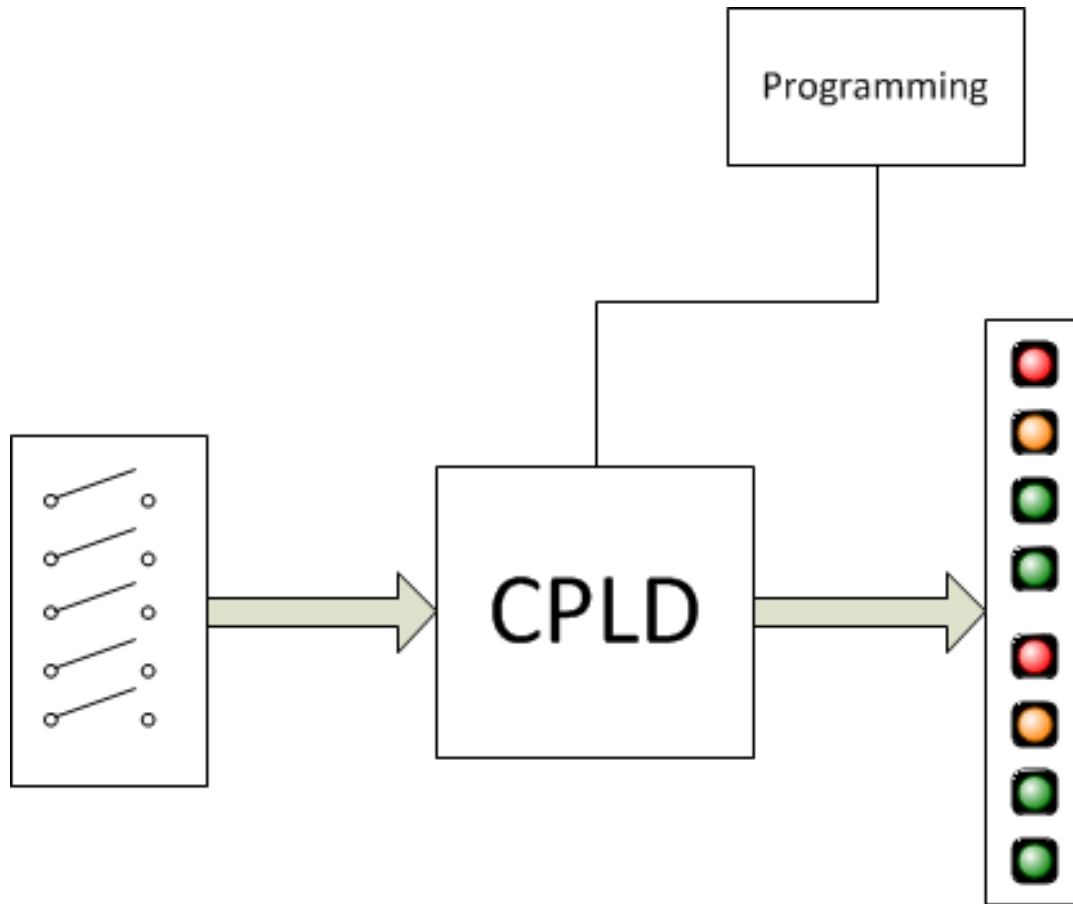
1984: First CPLD (Altera)

1985: First FPGA (Xilinx)

BORA THE BINARY EXPLORER



BORA ARCHITECTURE



XC9536XL CPLD SPECS

- Based on XC9500 family introduced in 1996
- 36 macrocells, 800 usable gates
- 5nS pin-to-pin delay
- Frequency up to 178 MHz

XC9500XL ARCHITECTURE

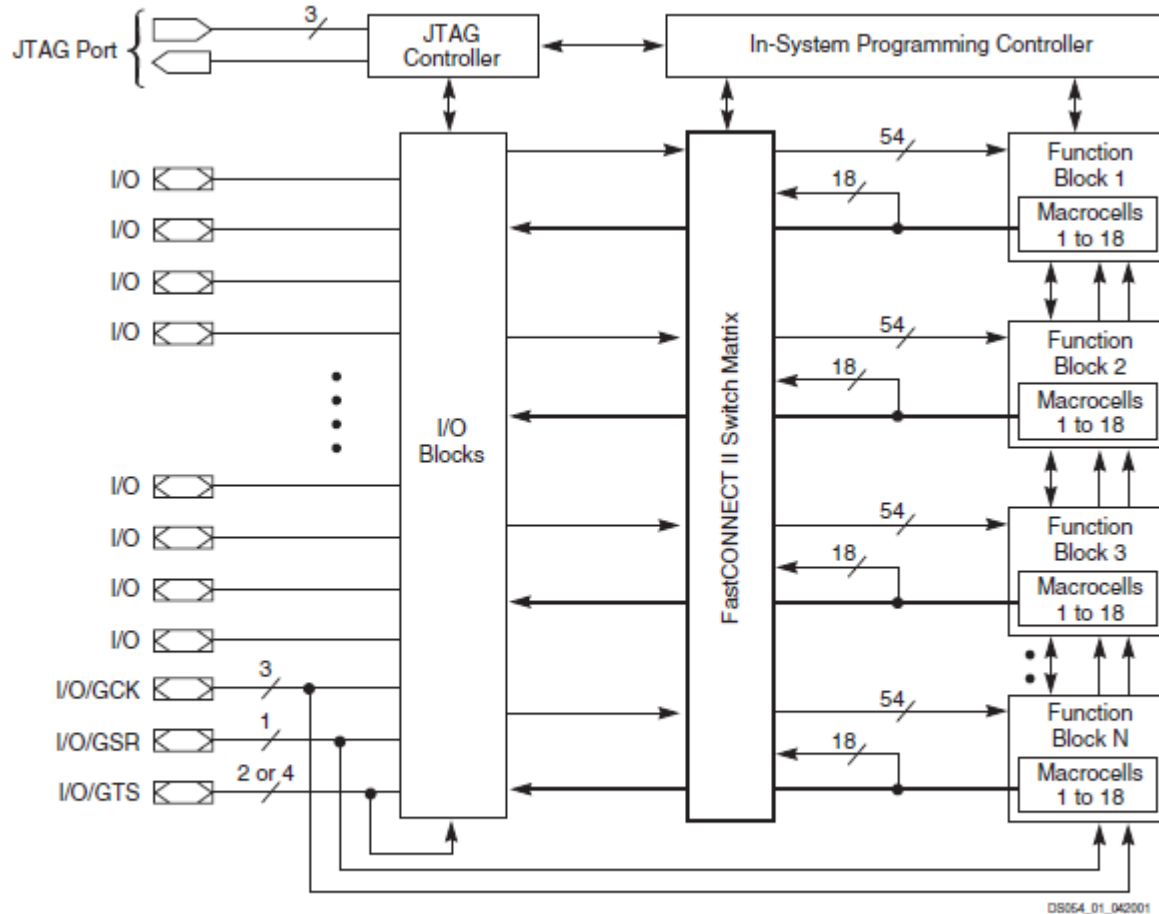
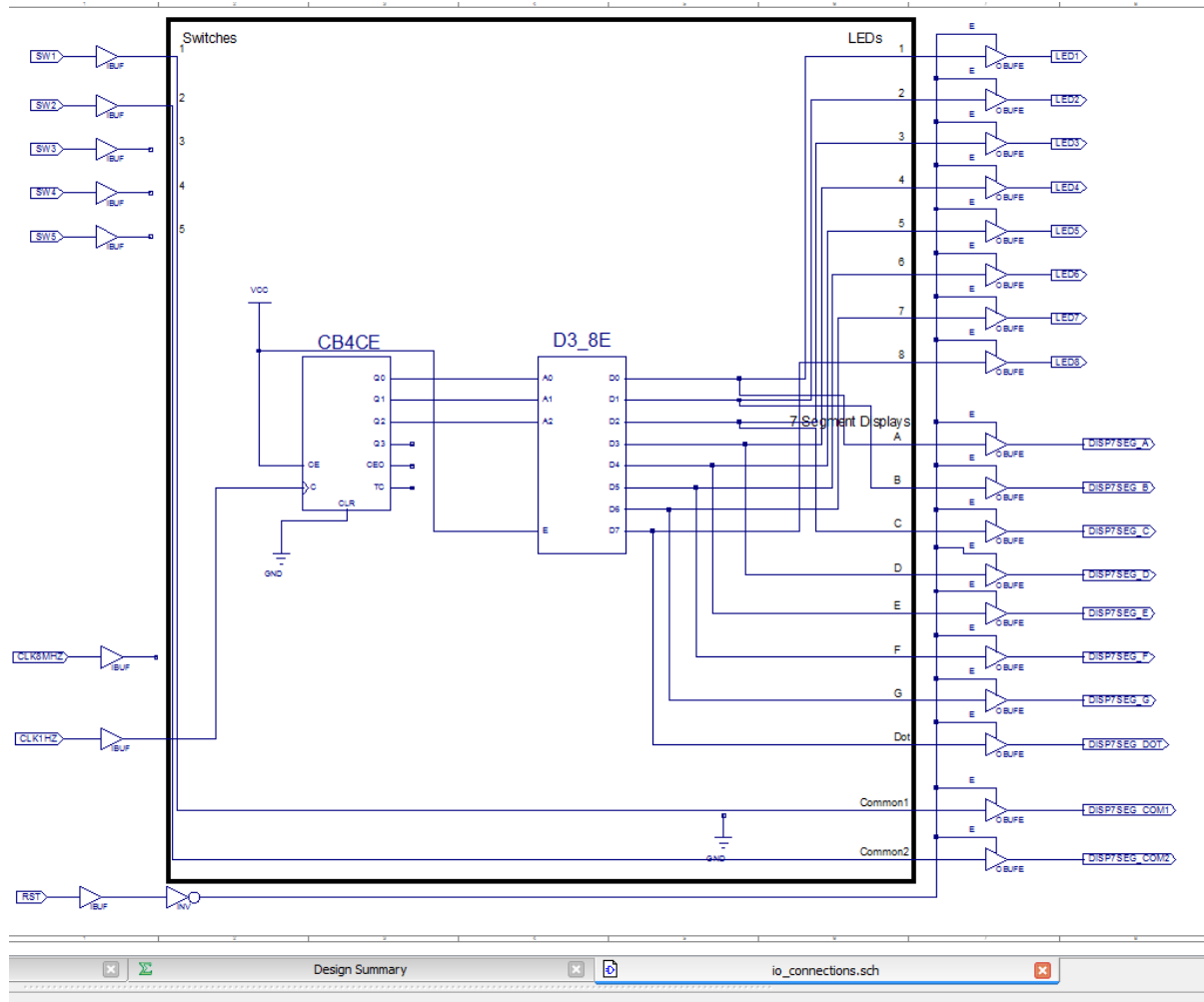


Figure 1: XC9500XL Architecture

Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

USING PROGRAMMABLE LOGIC: STEP 1



USING PROGRAMMABLE LOGIC: STEP 2

The screenshot shows the Xilinx ISE software interface. On the left, the 'Design' window displays a project hierarchy for 'DigitalTrainer_Simple' with files like 'xc9536xl-5VQ44', 'io_connections (io_connections.sch)', and 'DigitalTrainer_ConstraintsFile.ucf'. Below this, the 'Processes' window shows a list of steps including 'Synthesize - XST', 'Fit', and 'Generate Timing'. The main window displays the 'CPLD Reports' for the 'io_connections' design, with the 'Fitter Report' selected. The report includes a 'Summary' table, a 'RESOURCES SUMMARY' table, a 'PIN RESOURCES' table, and a 'GLOBAL RESOURCES' section.

XILINX CPLD Reports **XC9500XL**

Fitter Report | Timing Report

Fitter Report

Summary
Errors/Warnings
Logic
Inputs
Function Blocks
Equations
Pin List
Compiler Options
Text Report
Help

Equation Display Style
VHDL

No Processes Running

Processes: io_connections

- Design Summary/Reports
- Design Utilities
- User Constraints
- Implement Design
- Synthesize - XST
- Translate
- Fit
- Generate Programming File
- Configure Target Device
- Optional Implementation Tools
- Generate Timing
- Generate Post-Fit Simulation Model
- Generate IBIS Model
- Lock Pins

Summary

Design Name	io_connections
Fitting Status	Successful
Software Version	0.61xd
Device Used	XC9536XL-5-VQ44
Date	7-17-2012, 10:18PM

RESOURCES SUMMARY

Macrocells Used	Pterms Used	Registers Used	Pins Used	Function Block Inputs Used
21/36 (59%)	38/180 (22%)	3/36 (9%)	22/34 (65%)	10/108 (10%)

PIN RESOURCES

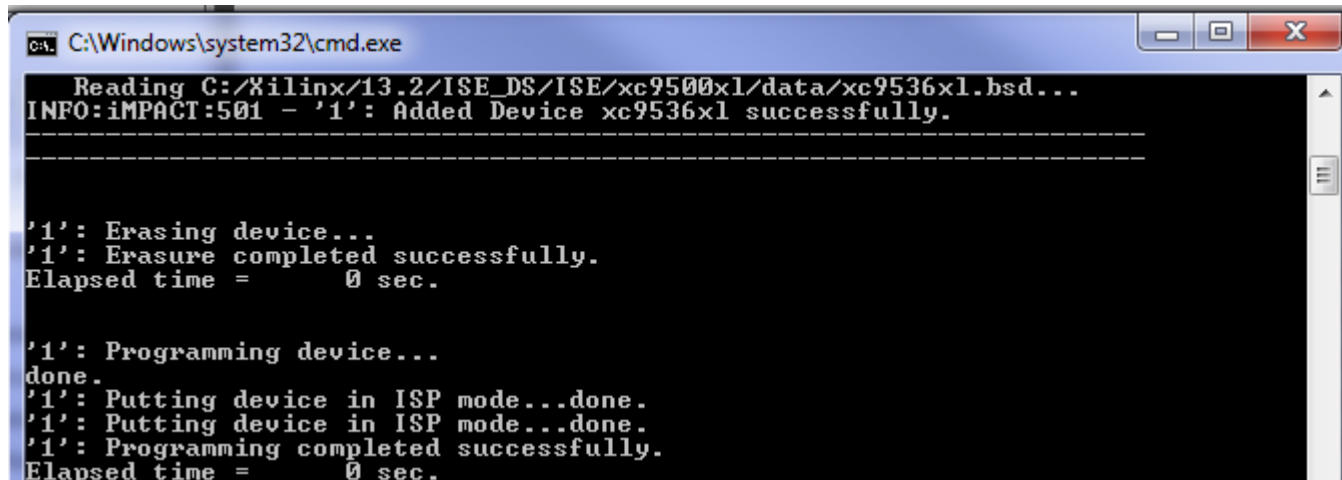
Signal Type	Required	Mapped	Pin Type	Used	Total
Input	3	3	I/O	18	29
Output	18	18	GCK/IO	1	3
Bidirectional	0	0	GTS/IO	2	2
GCK	1	1	GSR/IO	1	1
GTS	0	0			
GSR	0	0			

GLOBAL RESOURCES

Signal mapped onto global clock net (GCK2)	CLK1HZ
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POWER DATA

USING PROGRAMMABLE LOGIC: STEP 3



```
C:\Windows\system32\cmd.exe
Reading C:/Xilinx/13.2/ISE_DS/ISE/xc9500x1/data/xc9536x1.bsd...
INFO:iMPACT:501 - '1': Added Device xc9536x1 successfully.
-----
'1': Erasing device...
'1': Erasure completed successfully.
Elapsed time = 0 sec.

'1': Programming device...
done.
'1': Putting device in ISP mode...done.
'1': Putting device in ISP mode...done.
'1': Programming completed successfully.
Elapsed time = 0 sec.
```

CHOICE OF DESIGN ENTRY

- Schematic Based
- Language Based
 - Verilog
 - VHDL

RESOURCES

www.newae.com/teaching has links to BORA board

Lots of Verilog/VHDL tutorials (e.g.:
<http://www.fpga4fun.com> , <http://www.asic-world.com/verilog/veritut.html>)

Xilinx tools are totally free!