ECED2200 – Digital Circuits

Programmable Logic

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General Notes

- See updates to these slides: www.newae.com/teaching
- These slides licensed under 'Creative Commons Attribution-ShareAlike 3.0 Unported License'
- These slides are not the complete course – they are extended in-class
- You will find the following references useful, see www.newae.com/teaching for more information/links:
  - The book "Bebop to the Boolean Boogie" which is available to Dalhousie Students
  - Course notes (covers almost everything we will discuss in class)
  - Various websites such as e.g.: www.play-hookey.com
  - The book "Contemporary Logic Design", which was used in previous iterations of the class and you may have already

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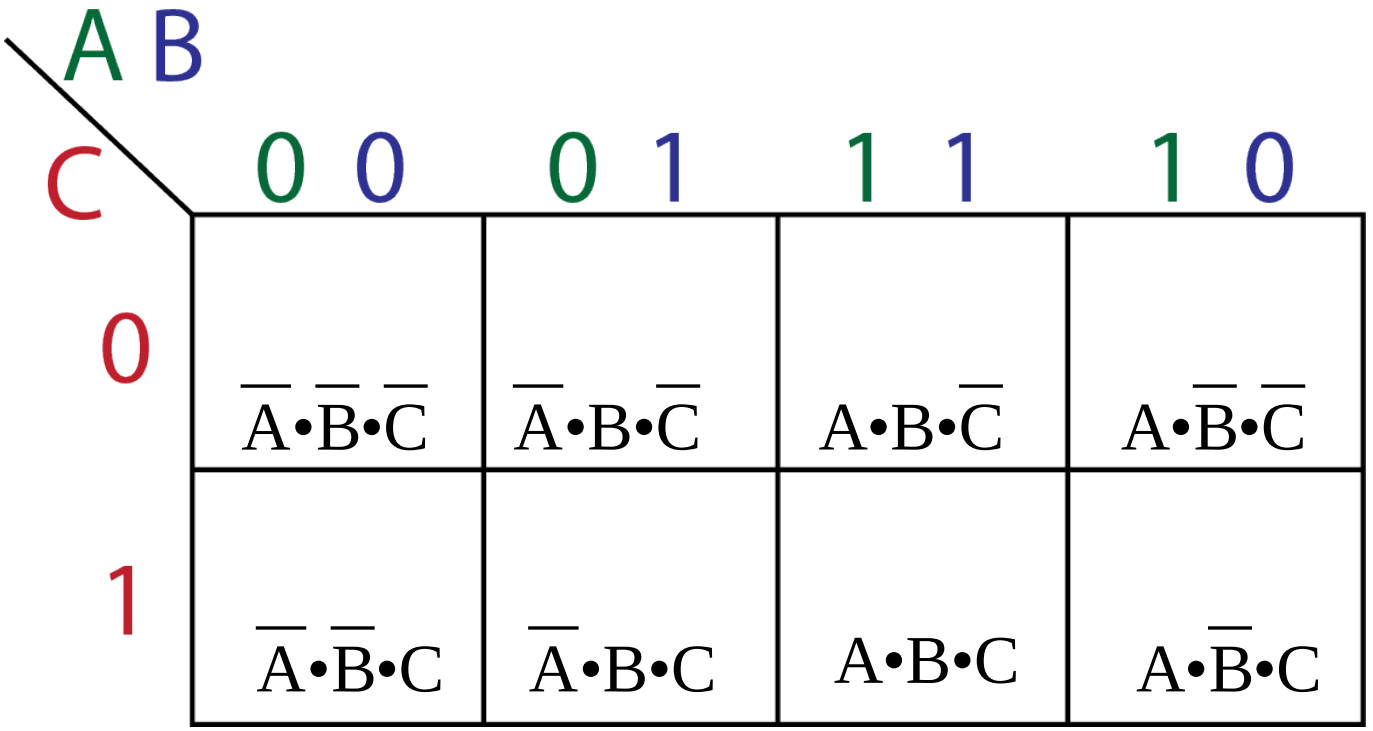
Implementing Designs



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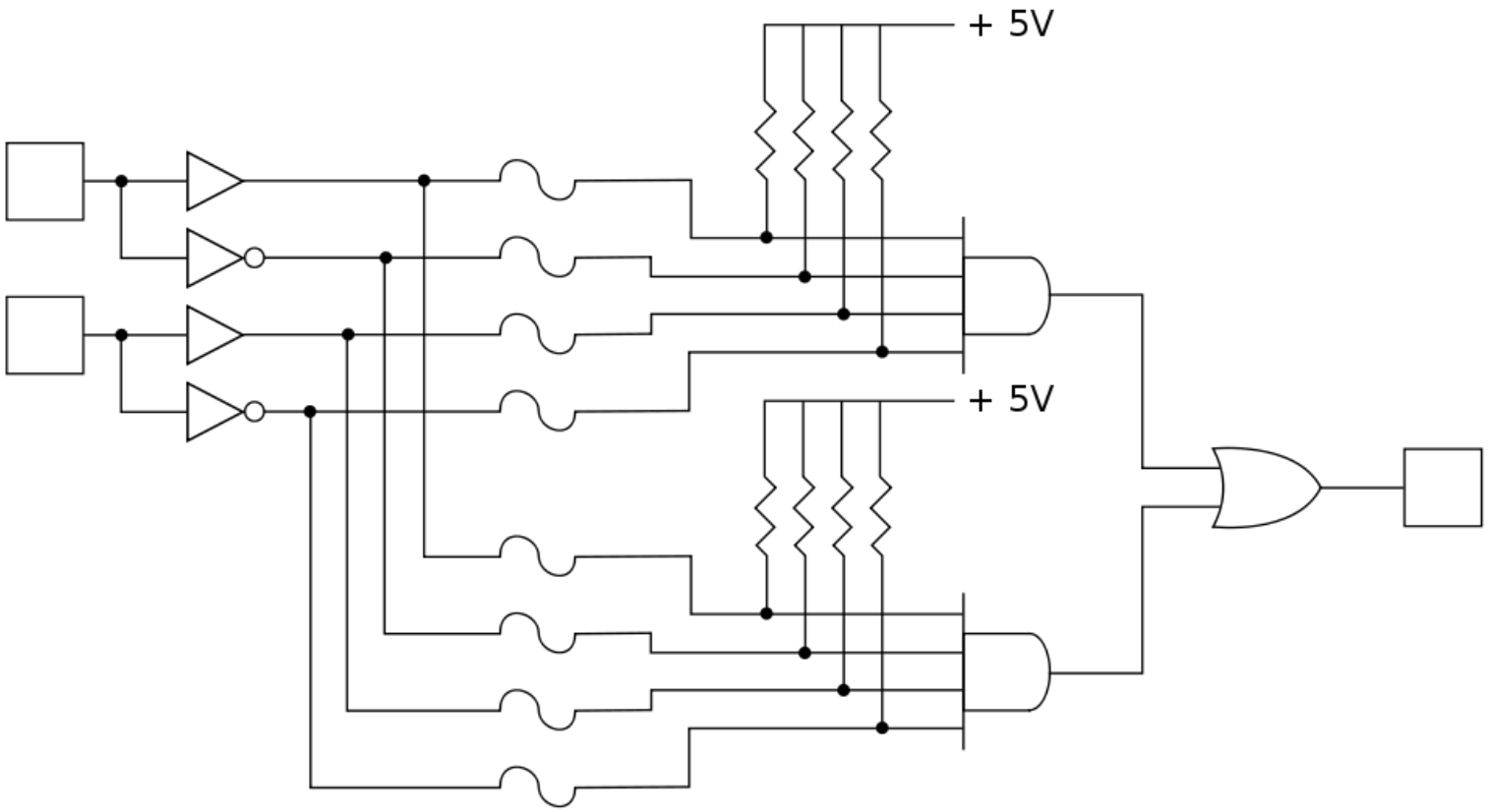
Programmable Array Logic (PAL)



Simplified programmable logic device

Source: http://en.wikipedia.org/wiki/File:Programmable_Logic_Device.svg

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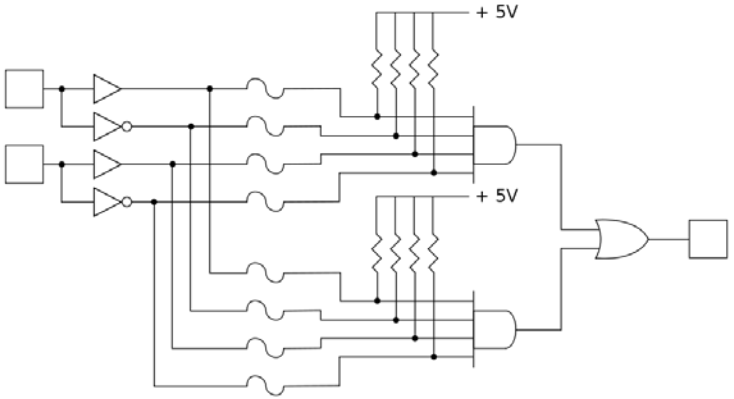
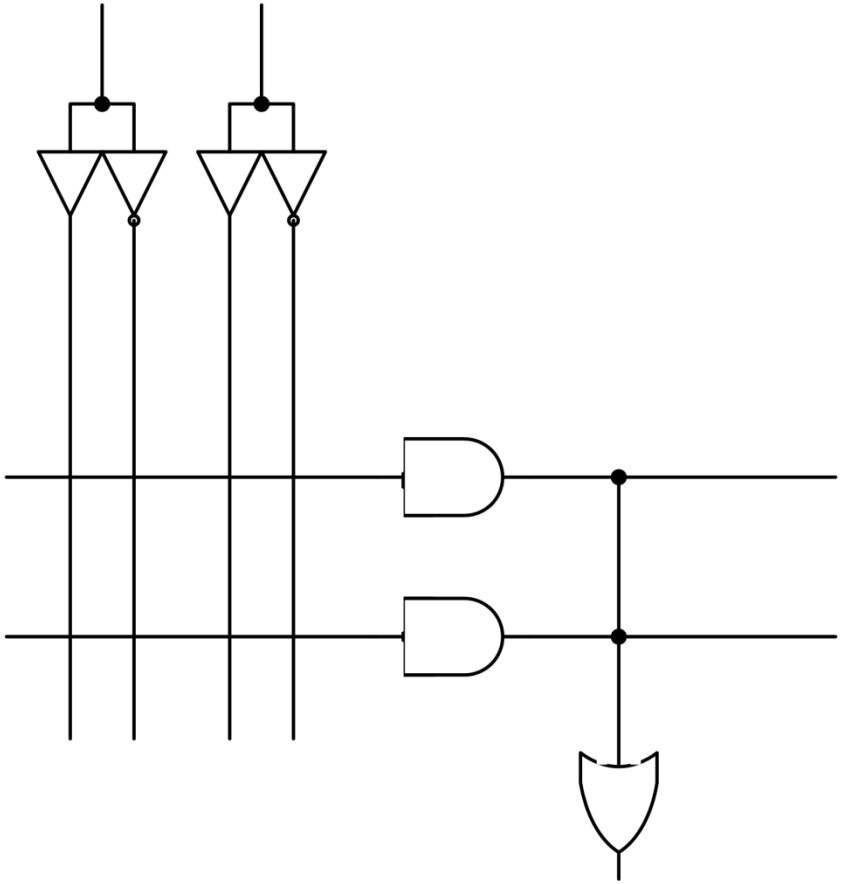
Programmable Array Logic (PAL)



Simplified programmable logic device



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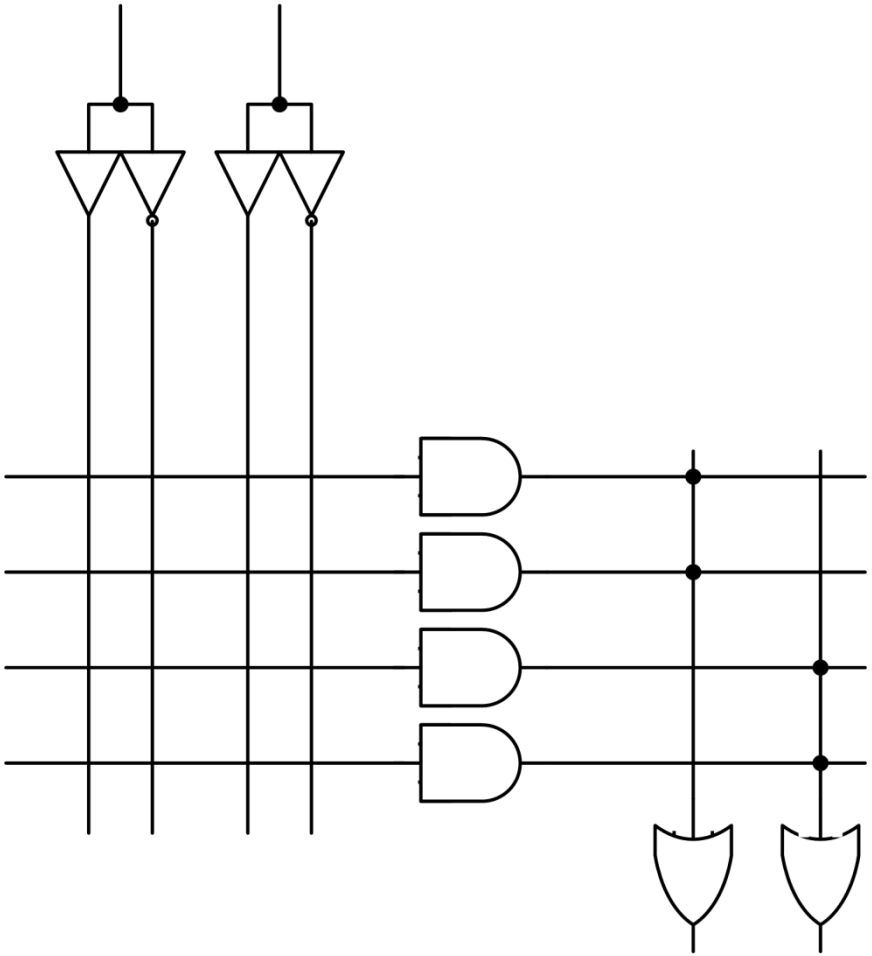
Programmable Array Logic



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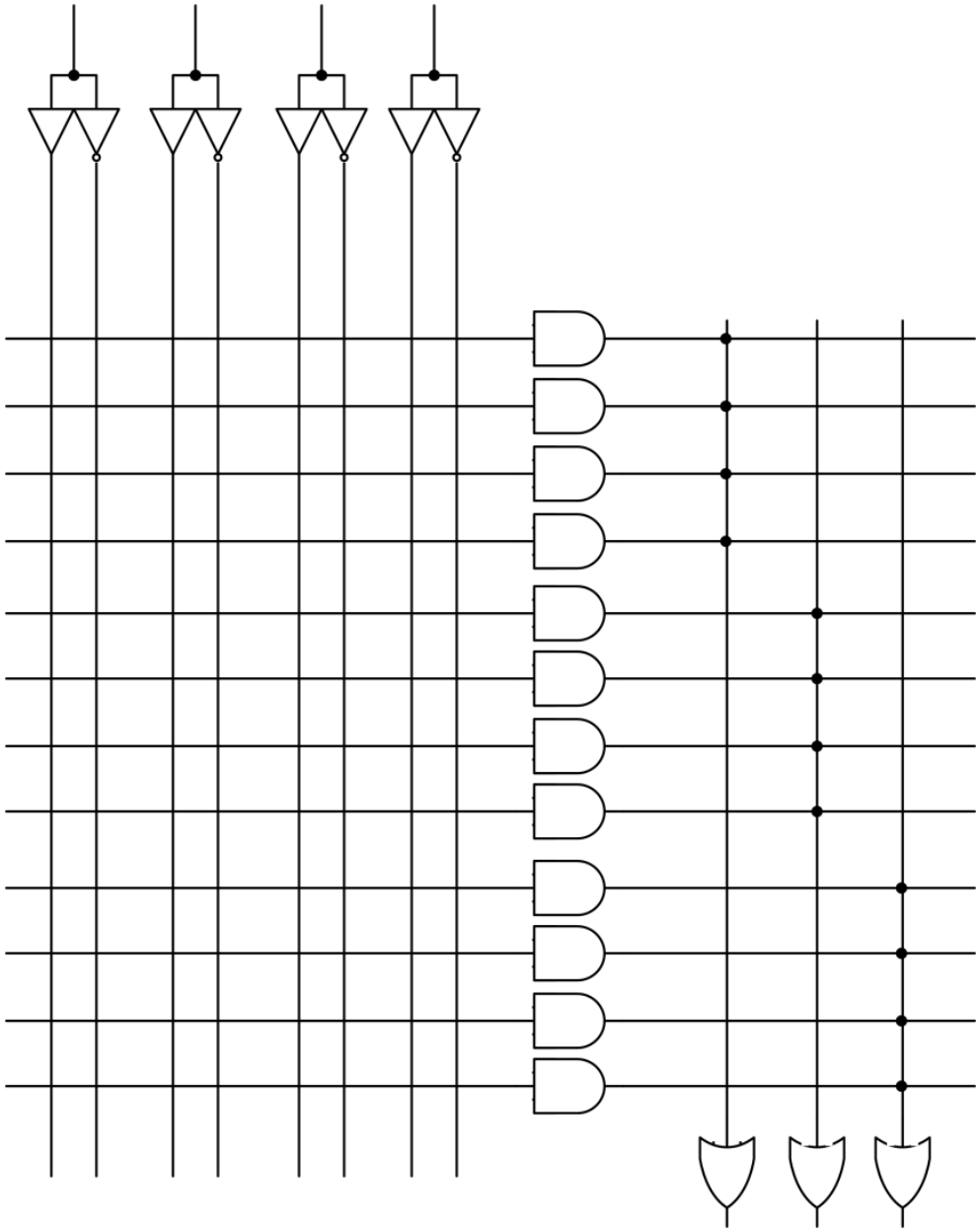

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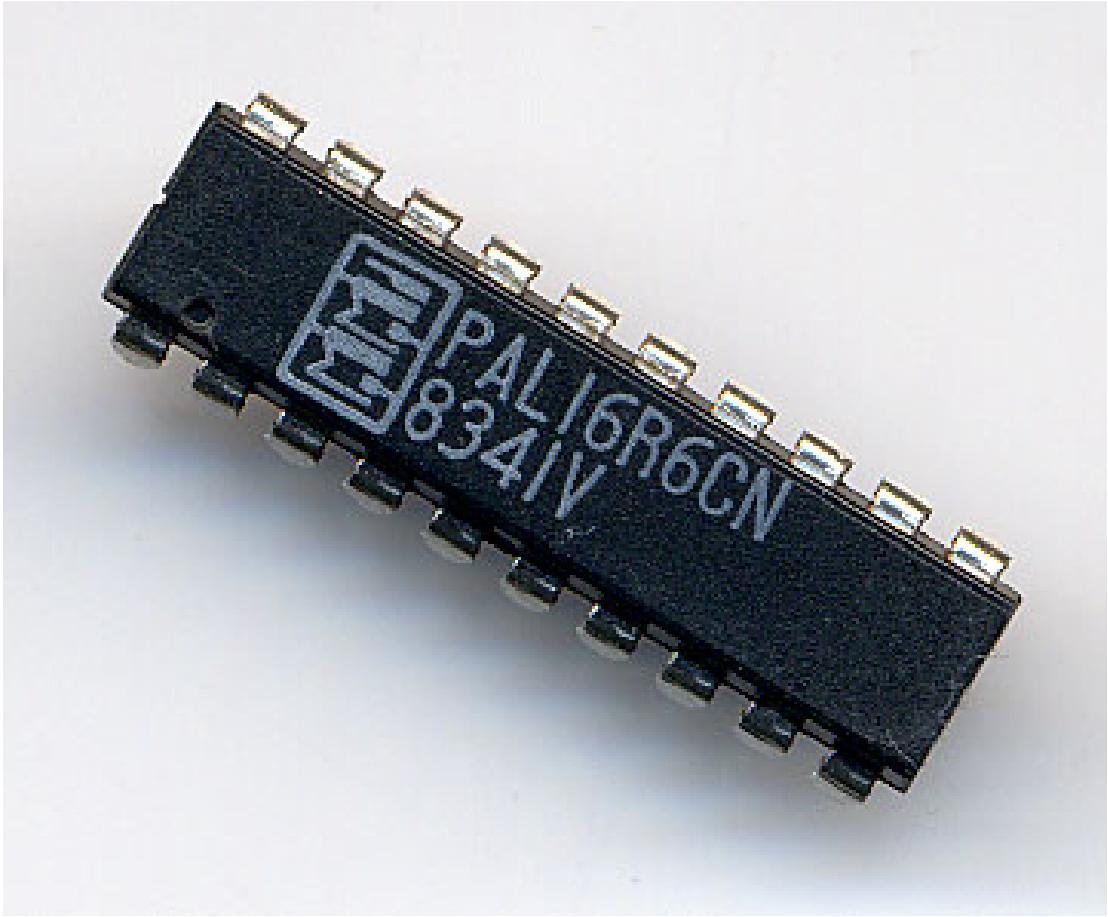

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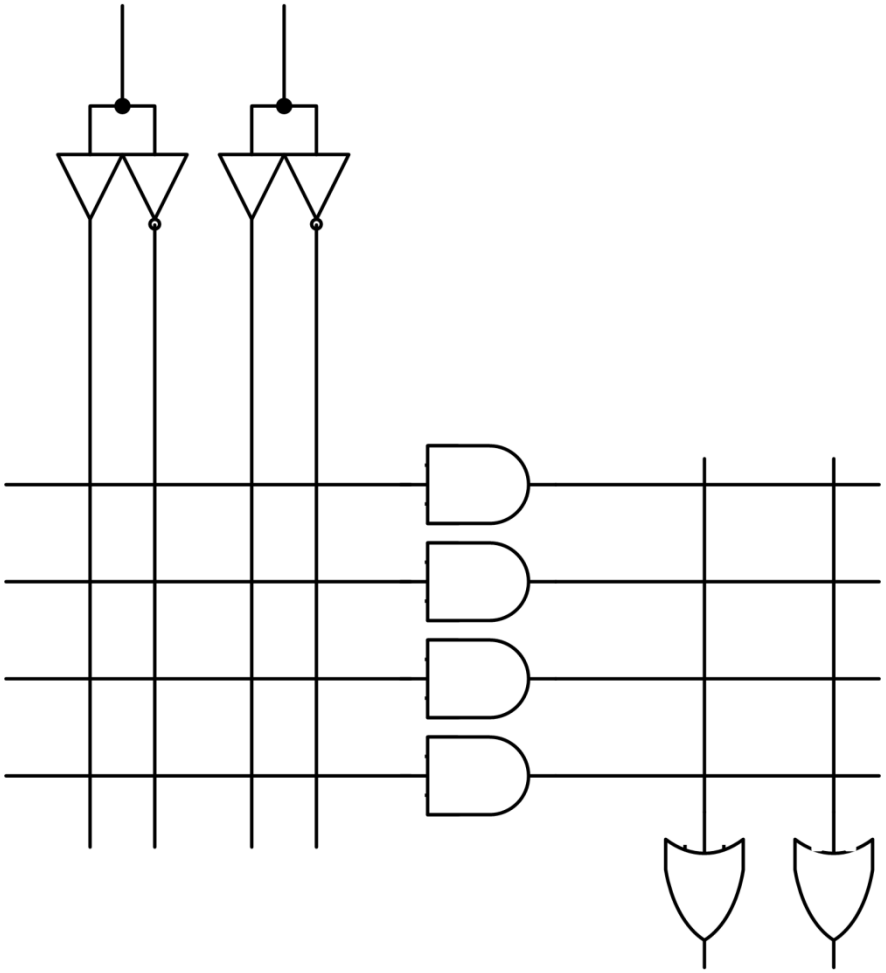
Programmable Logic Array (PLA)



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PAL vs PLA

PAL = AND inputs fused, OR inputs fixed

PLA = AND inputs fused, OR inputs fused

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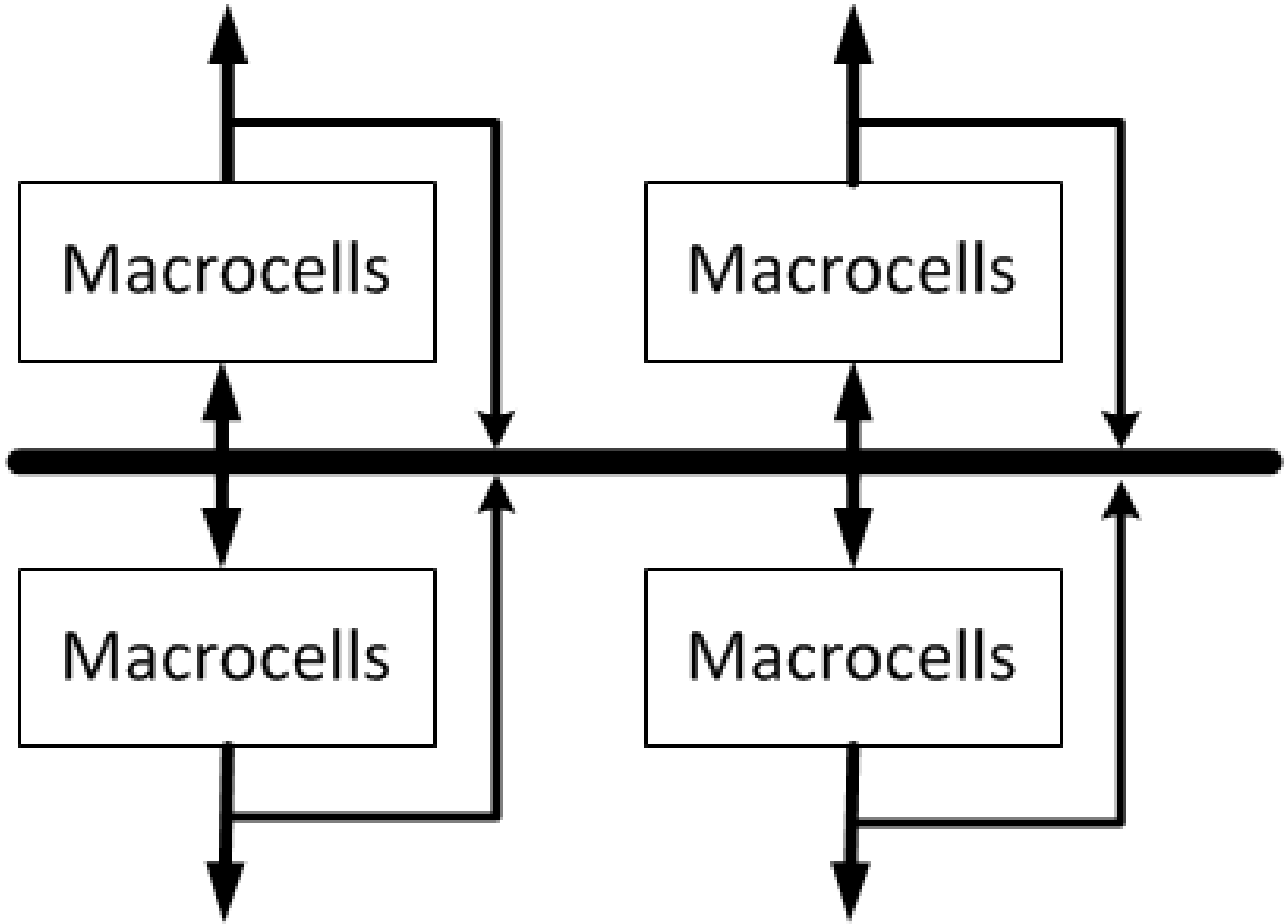
Complex Programmable Logic Devices



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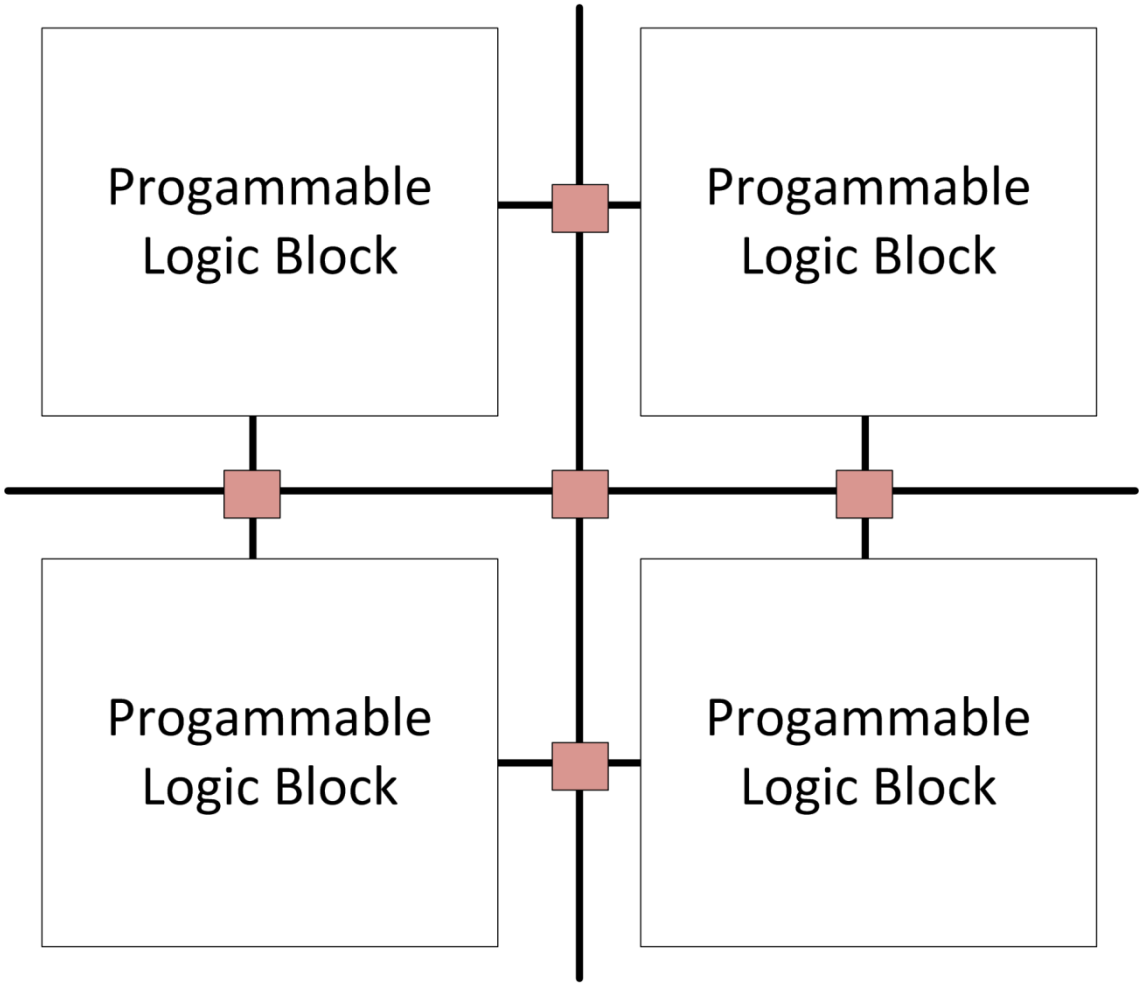
Field Programmable Gate Arrays



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Timeline

1975: First PLAs become available

1978: First PAL (MMI)

1983: First GAL (Lattice Semi)

1984: First CPLD (Altera)

1985: First FPGA (Xilinx)

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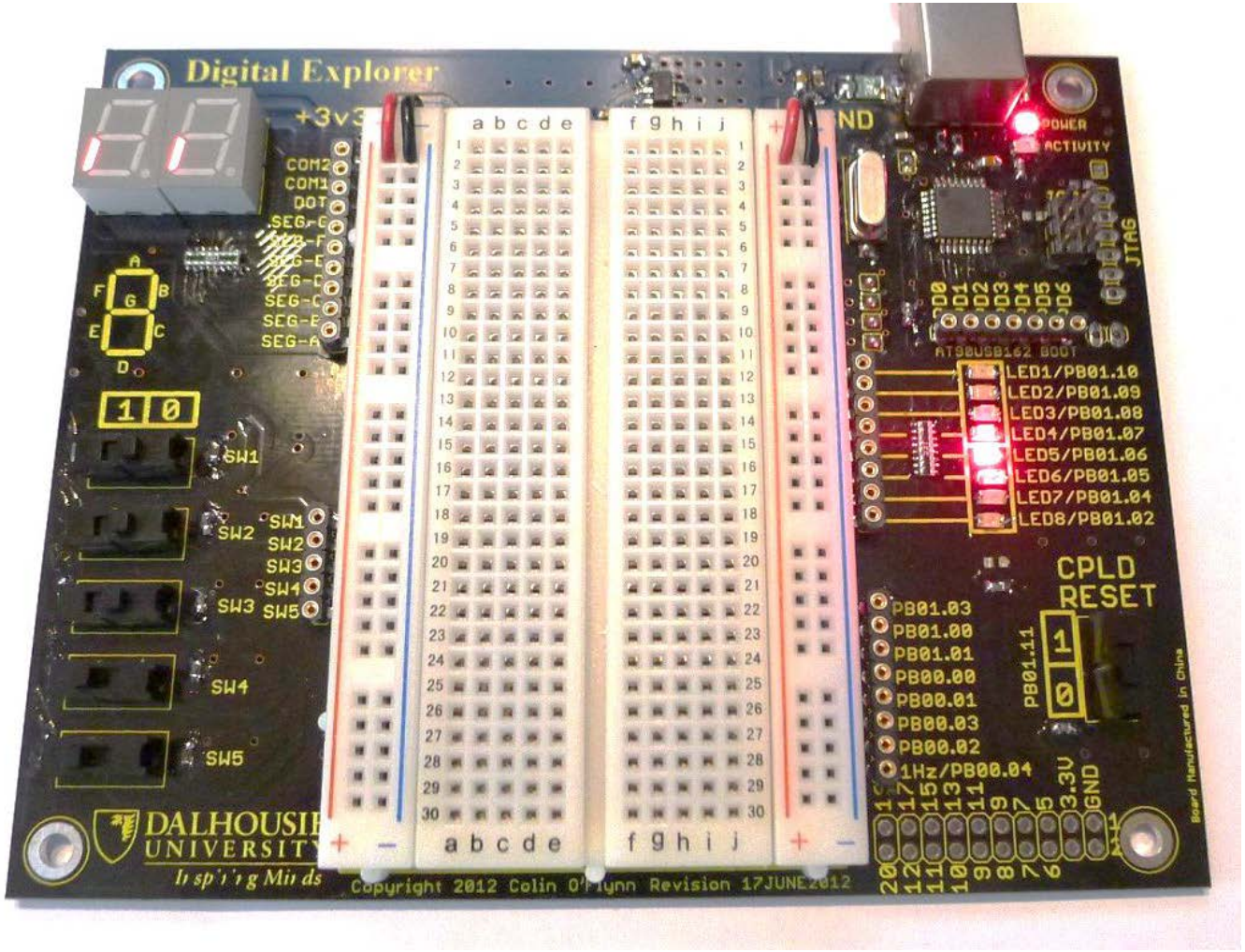
BORA the Binary Explorer



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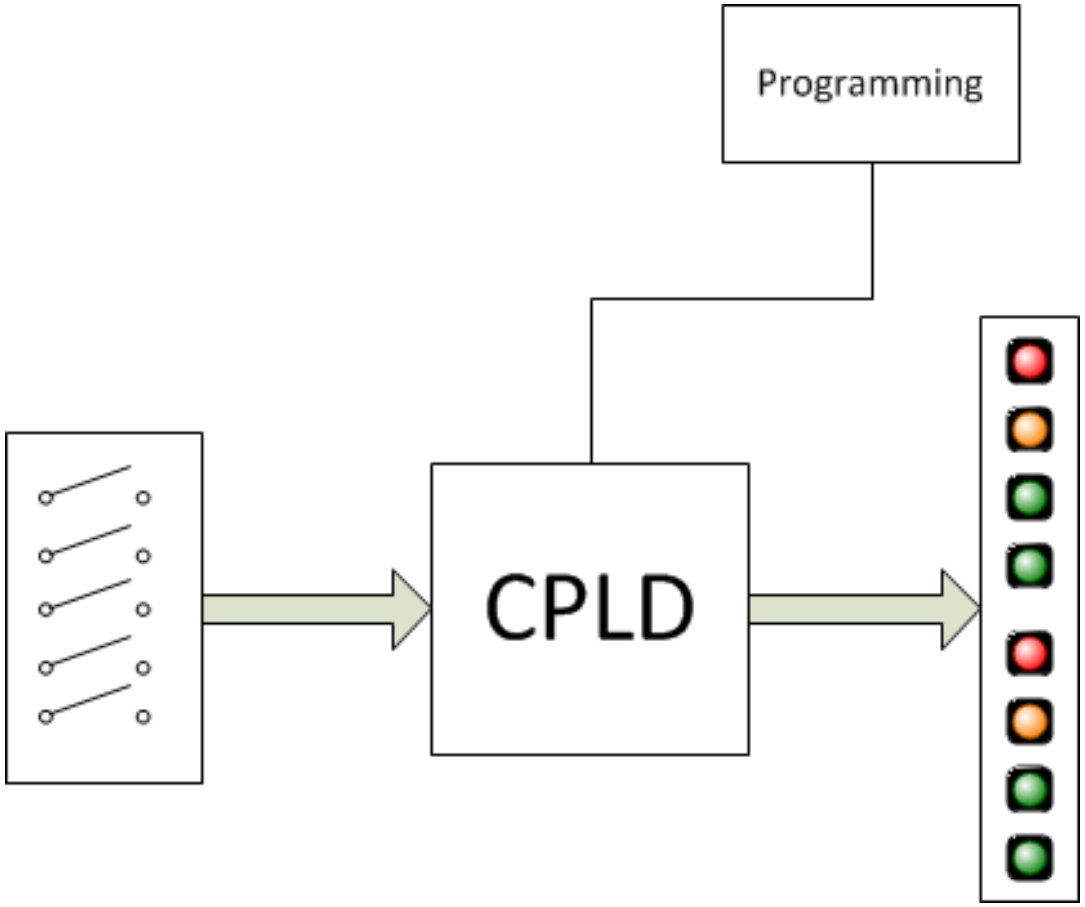
Bora Architecture



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XC9536XL CPLD Specs

- Based on XC9500 family introduced in 1996
- 36 macrocells, 800 usable gates
- 5nS pin-to-pin delay
- Frequency up to 178 MHz

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XC9500XL Architecture

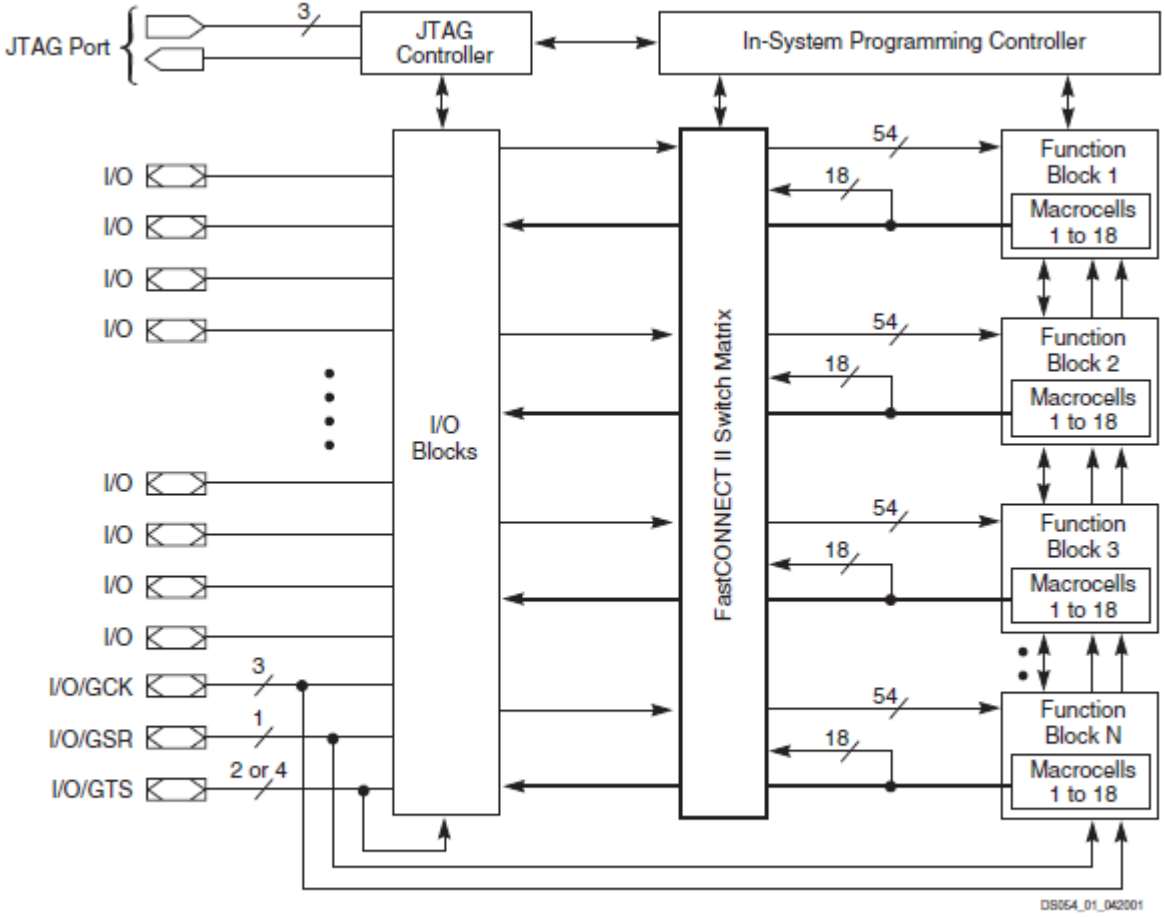

Figure 1: **XC9500XL Architecture**
Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

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XC9500XL Macrocells

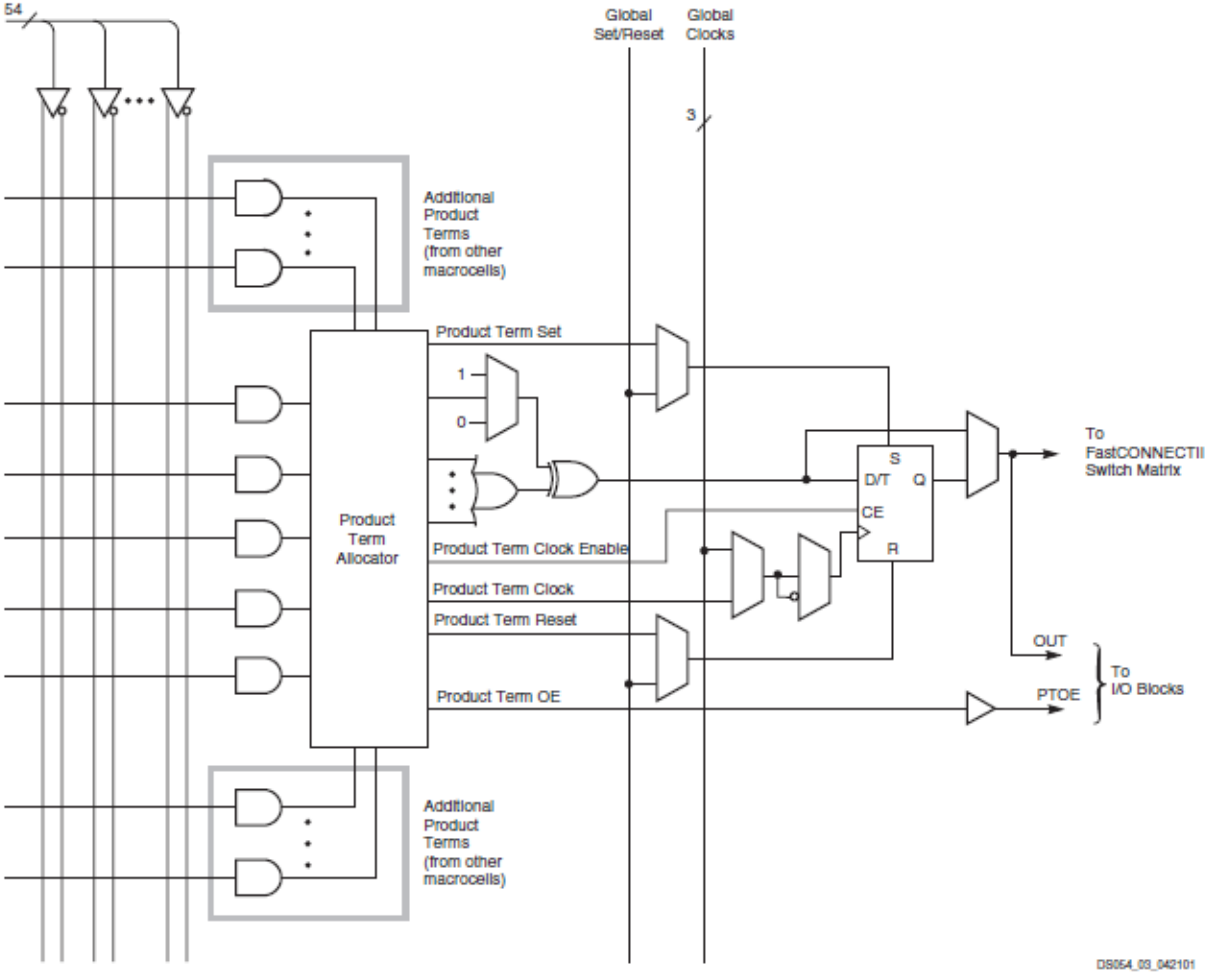
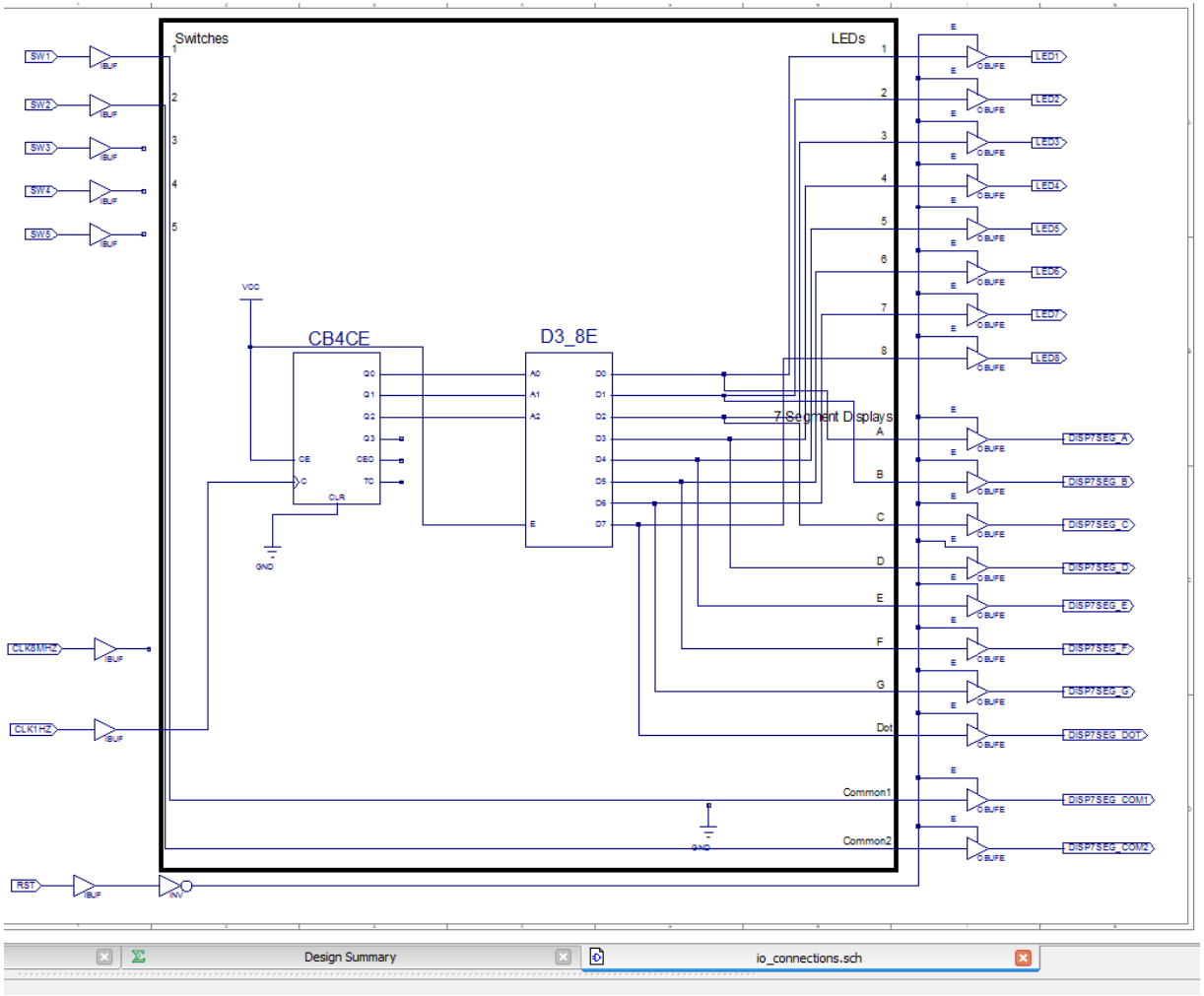


Figure 3: **XC9500XL Macrocell Within Function Block**

Using Programmable Logic: Step 1



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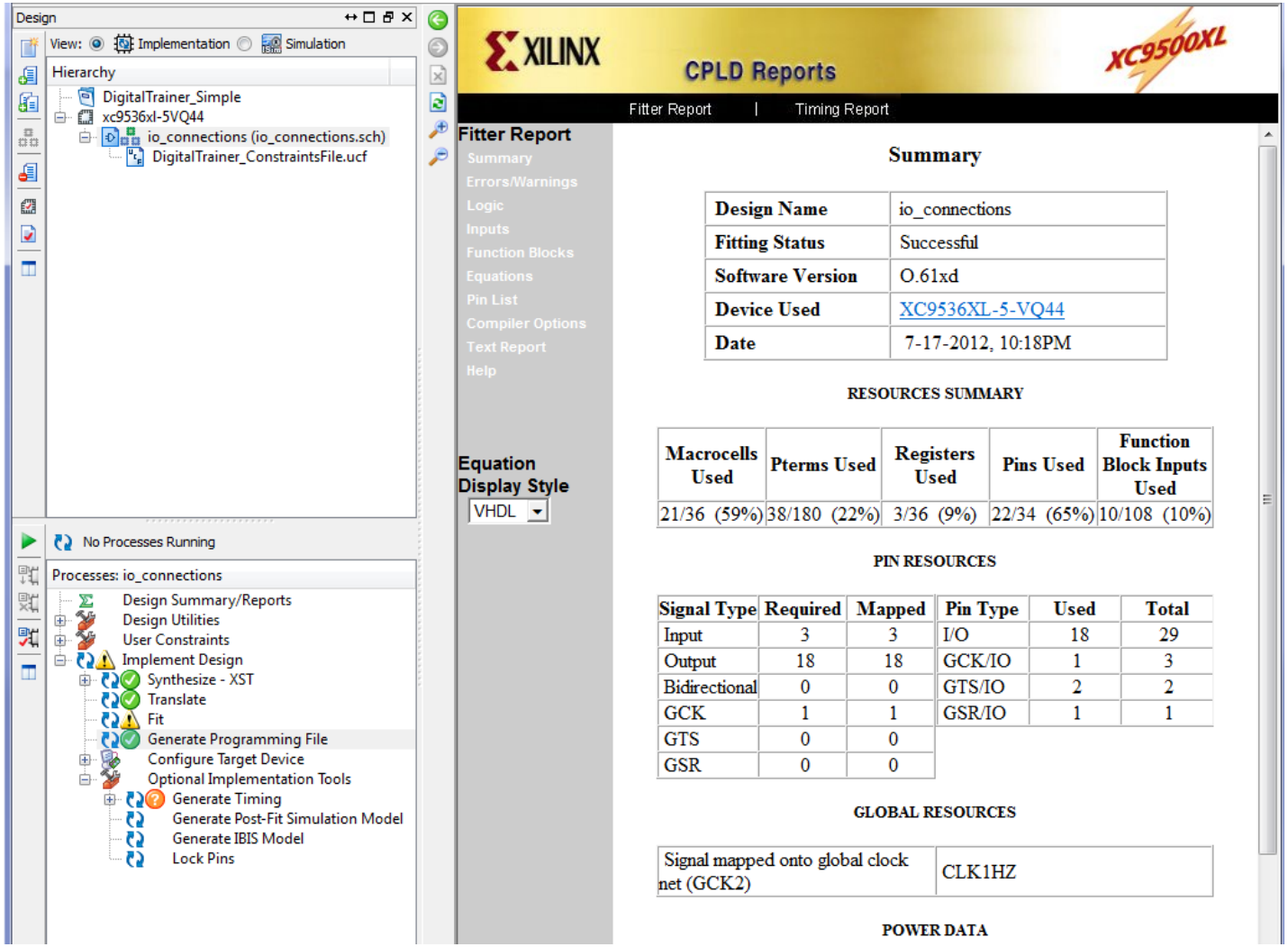
Using Programmable Logic: Step 2



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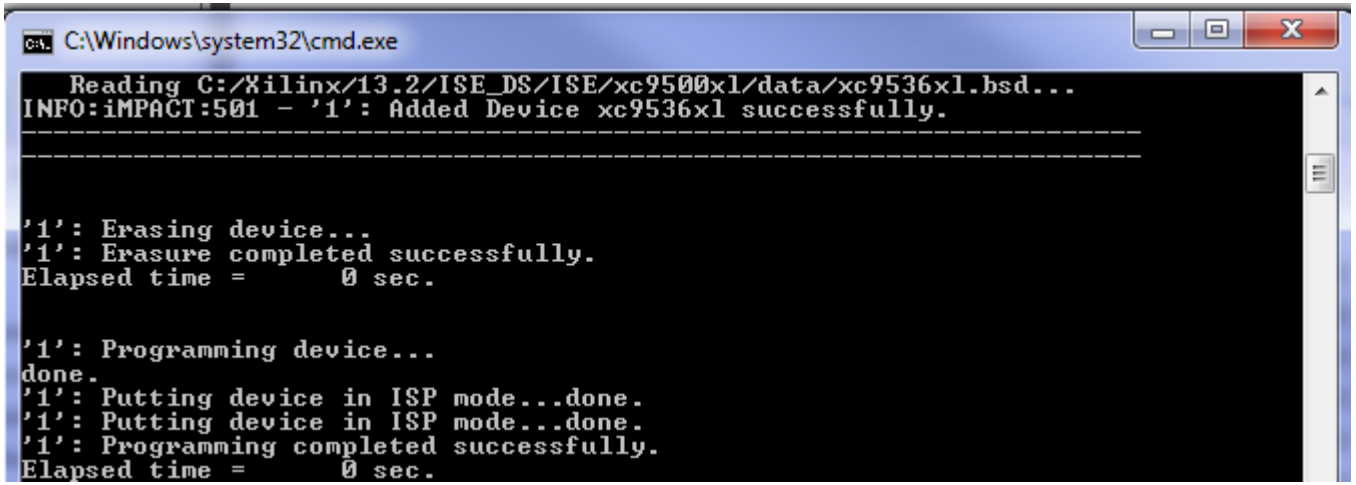
Using Programmable Logic: Step 3



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Choice of Design Entry

- Schematic Based

- Language Based
  - Verilog
  - VHDL

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Resources

www.newae.com/teaching has links to BORA board

Lots of Verilog/VHDL tutorials (e.g.: http://www.fpga4fun.com , http://www.asic-world.com/verilog/veritut.html)

Xilinx tools are totally free!

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