ECED2200 – Digital Circuits

Multiplexor & Demultiplexor

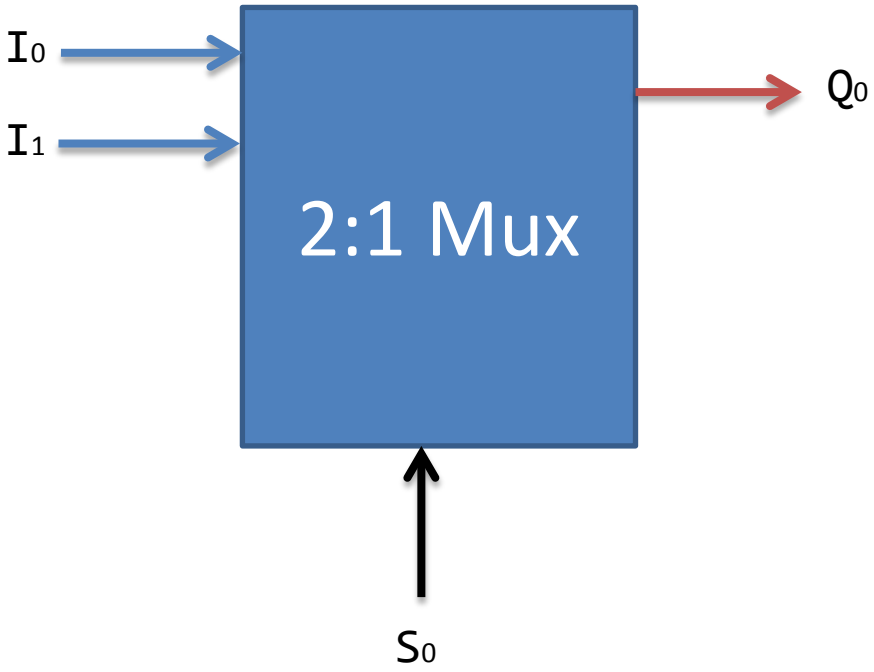
General Notes

- See updates to these slides: www.newae.com/teaching
- These slides licensed under 'Creative Commons Attribution-ShareAlike 3.0 Unported License'
- These slides are not the complete course – they are extended in-class
- You will find the following references useful, see www.newae.com/teaching for more information/links:
  - The book "Bebop to the Boolean Boogie" which is available to Dalhousie Students
  - Course notes (covers almost everything we will discuss in class)
  - Various websites such as e.g.: www.play-hookey.com
  - The book "Contemporary Logic Design", which was used in previous iterations of the class and you may have already

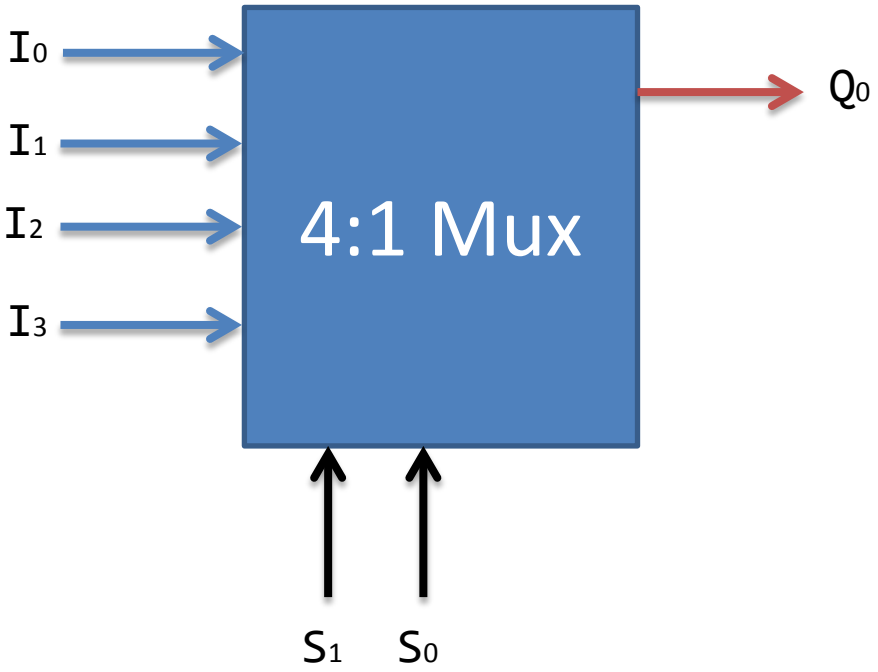
Multiplexor/Demultiplexor

What is a Multiplexor?

2:1 Mux



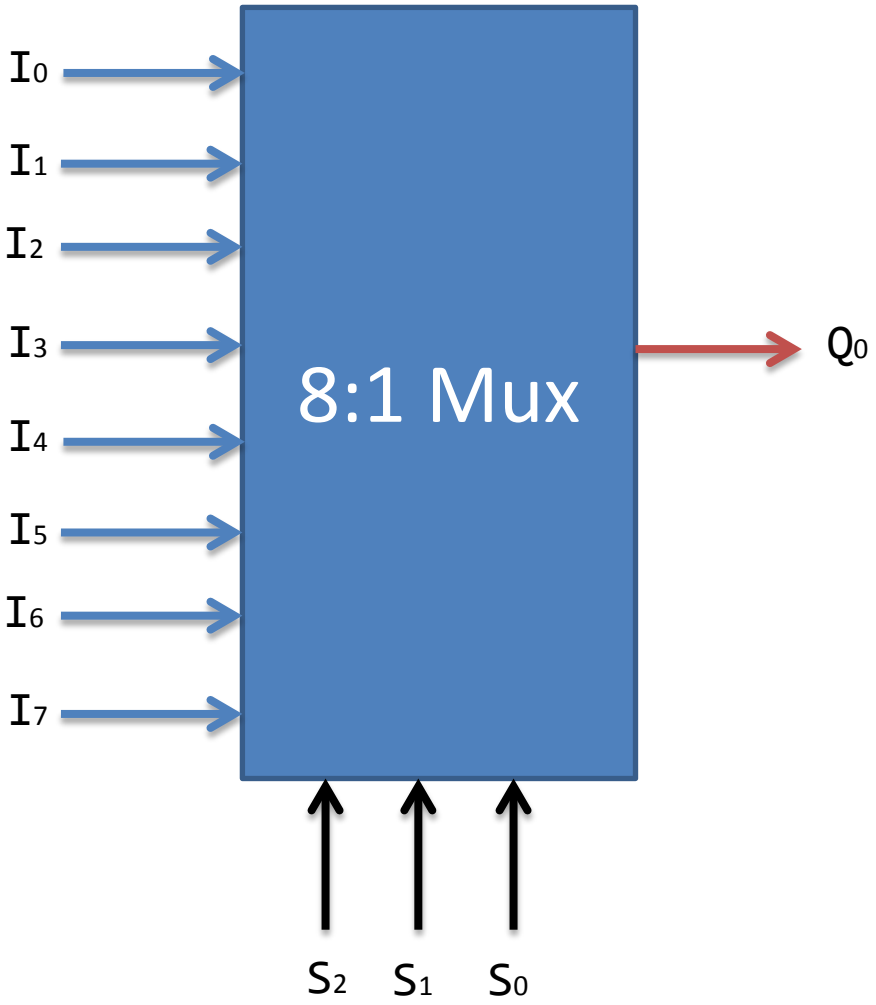
4:1 Mux



Equations of Mux

S1	S0	Q0
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

8:1 Mux

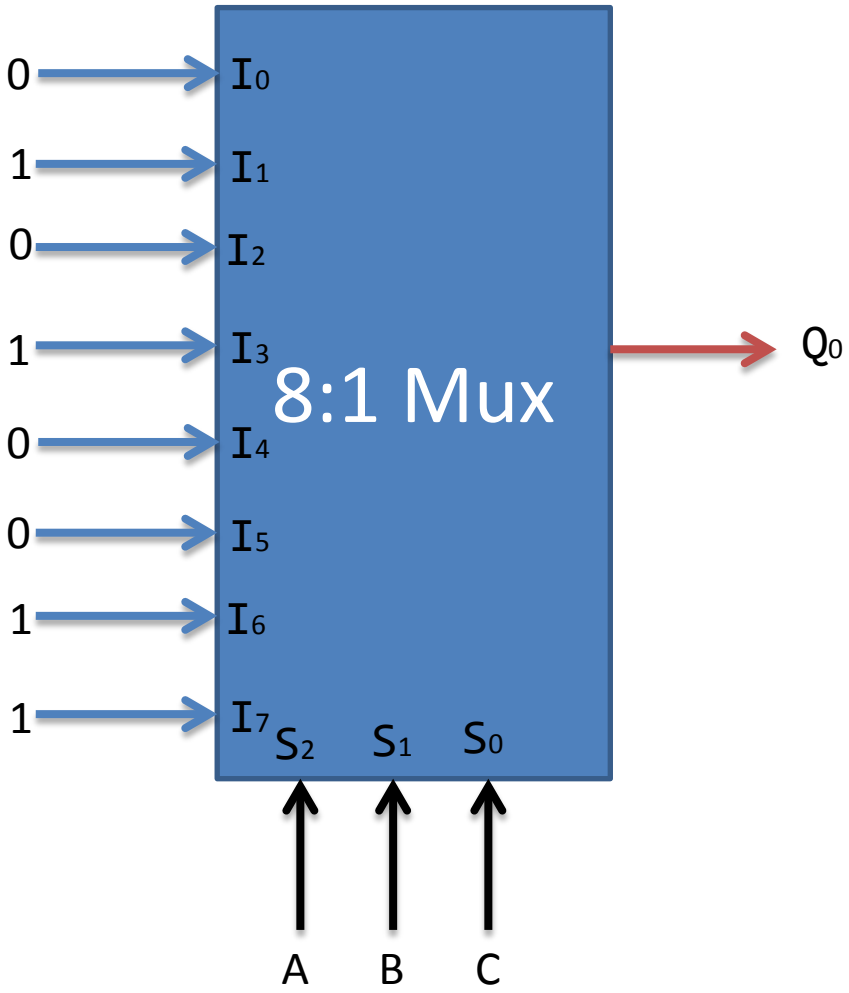


Mux as Design Block

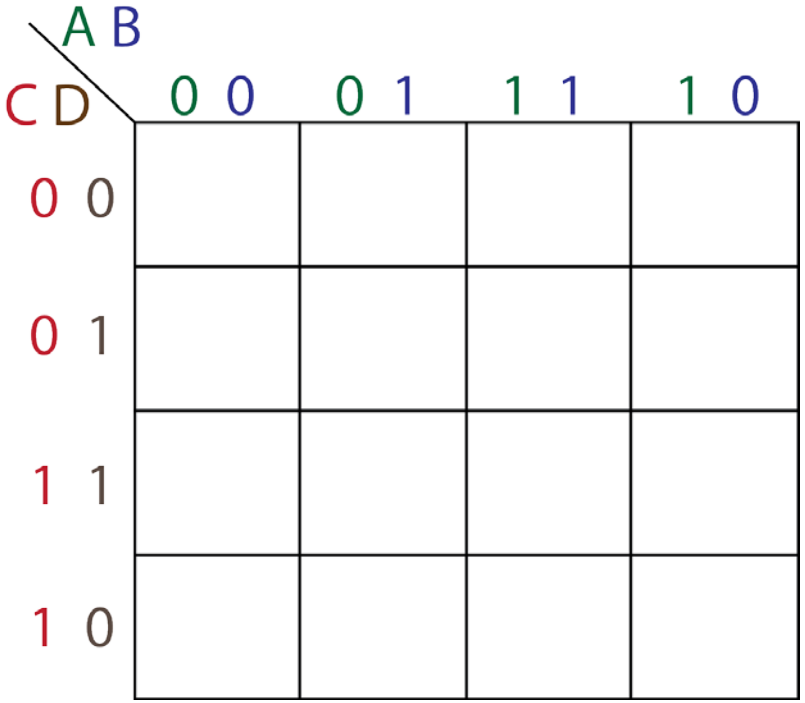
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

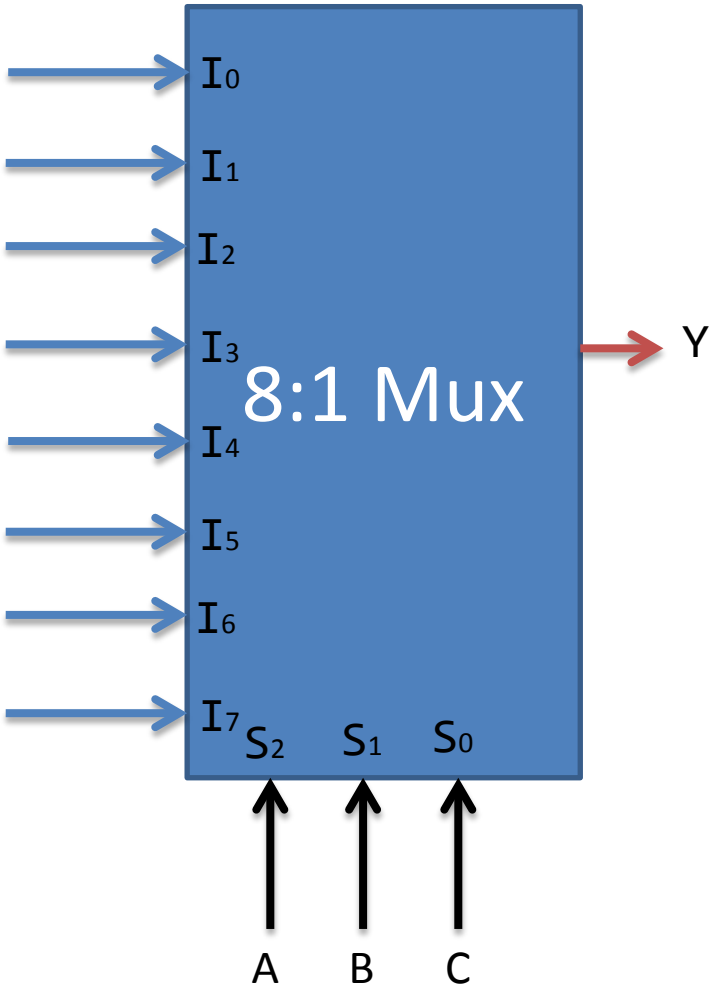
Mux as Design Block

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



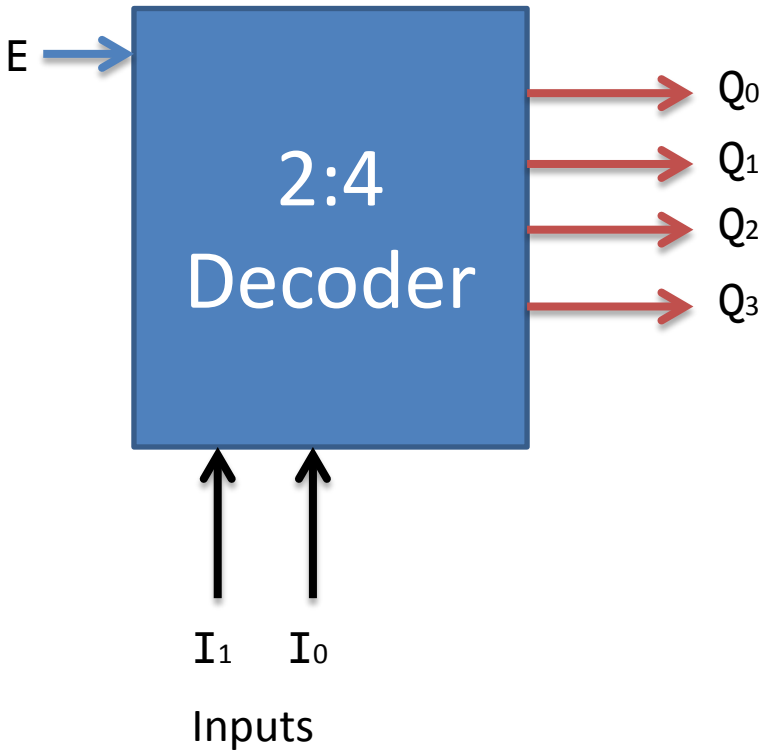
Mux as a Design Block

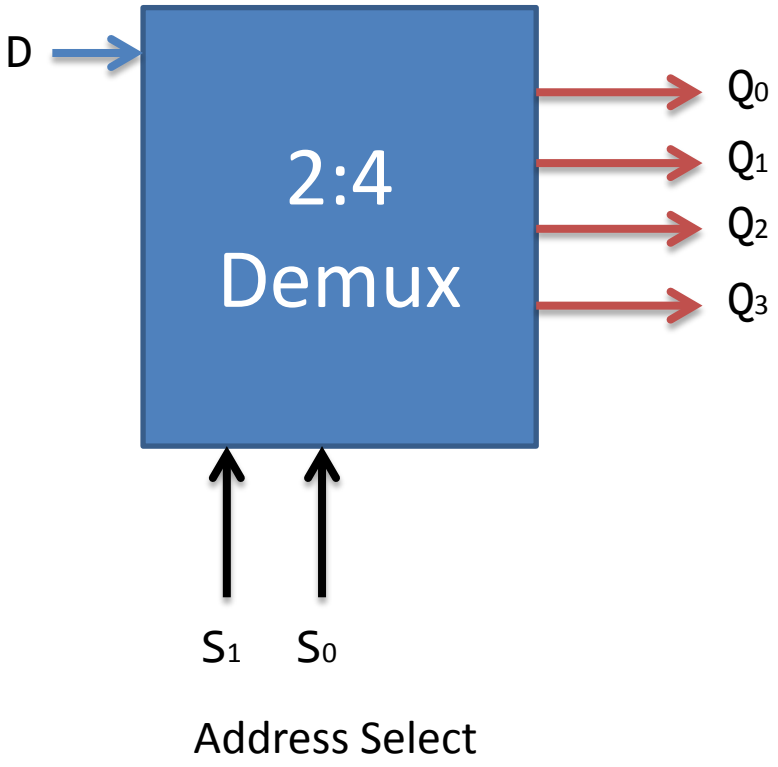




What is a Demultiplexor?

2:4 Decoder / Demux

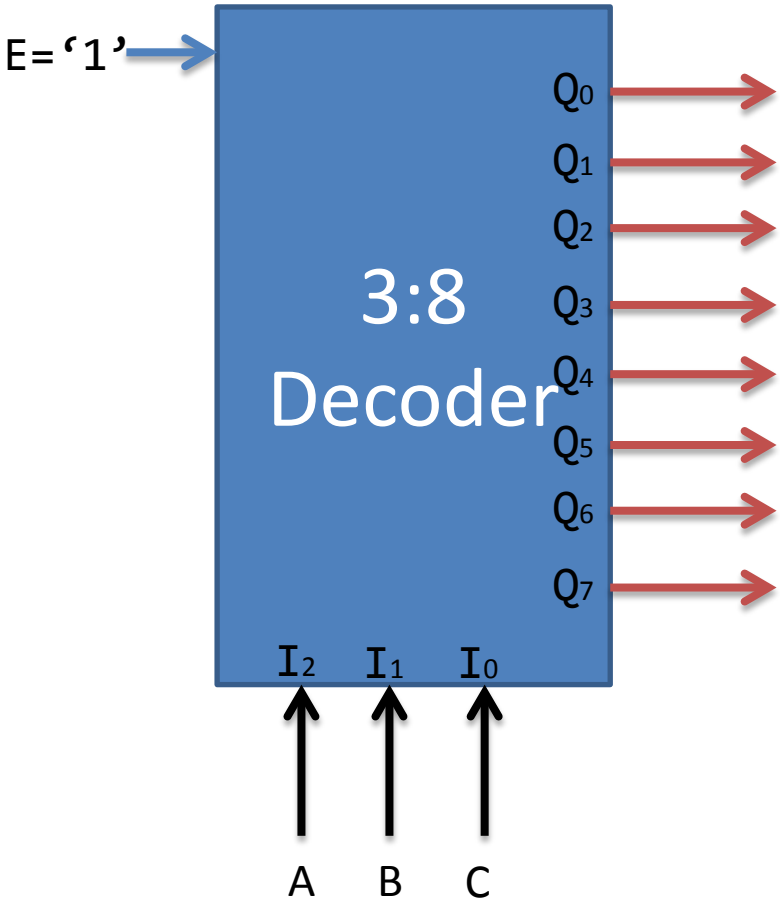




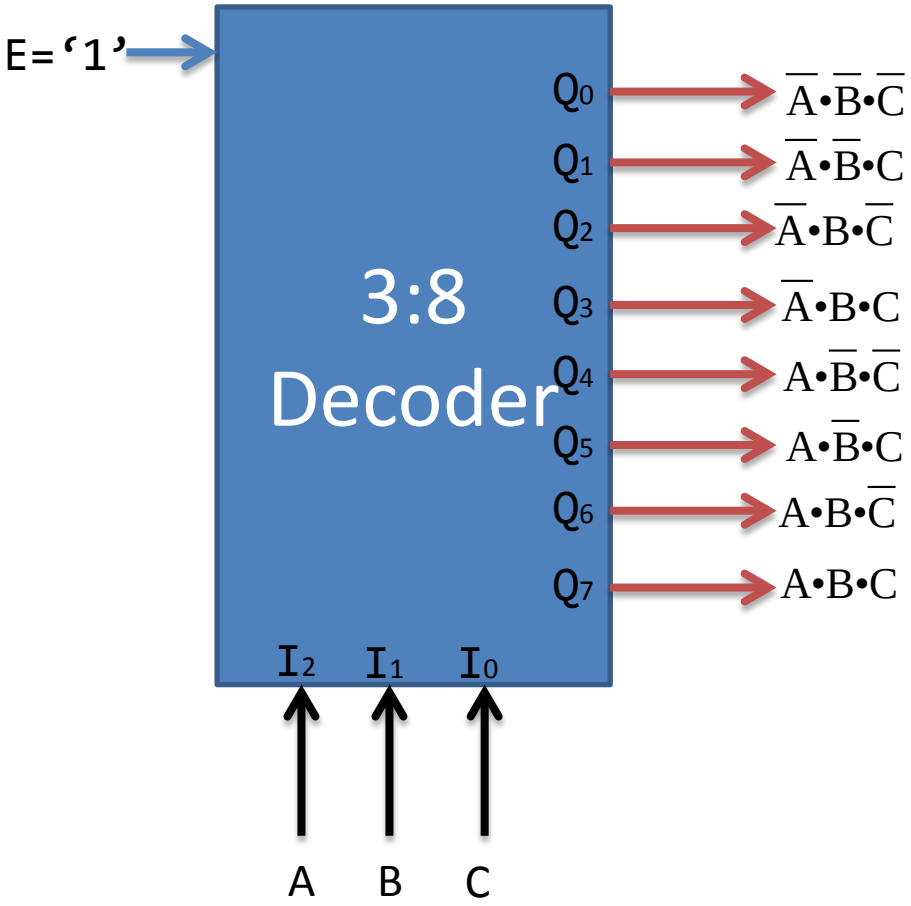
Notation Information

- When using ‘Enable’ (tie to ‘1’), we have a *decoder*. When inputting data, we have *demultiplexor (demux)*.
- Naming:
  - Decoder/demux named by “control signals:outputs” (e.g.: 2:4)
  - Mux named by “inputs:outputs” (e.g.: 4:1)

Decoder as a Design Block

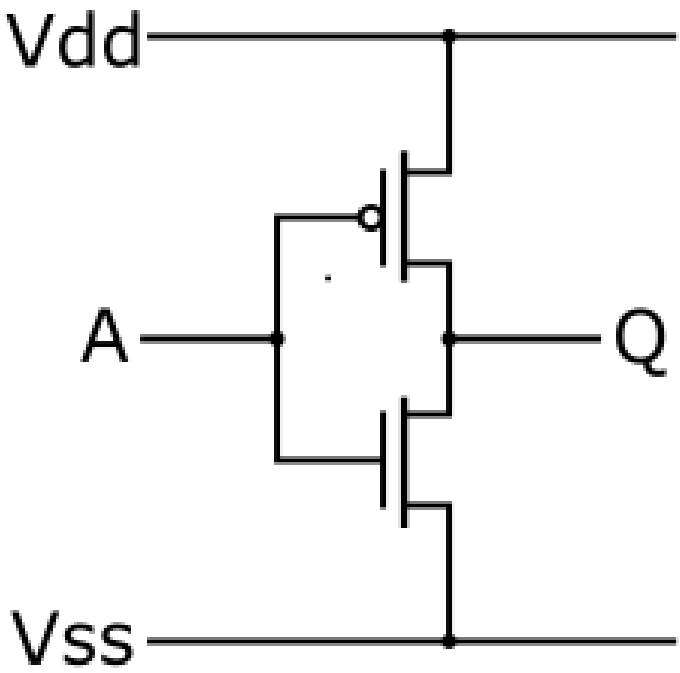


Decoder as a Minterm Generator

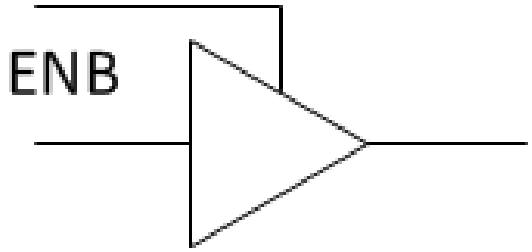


TRI-STATE GATES

Inverter

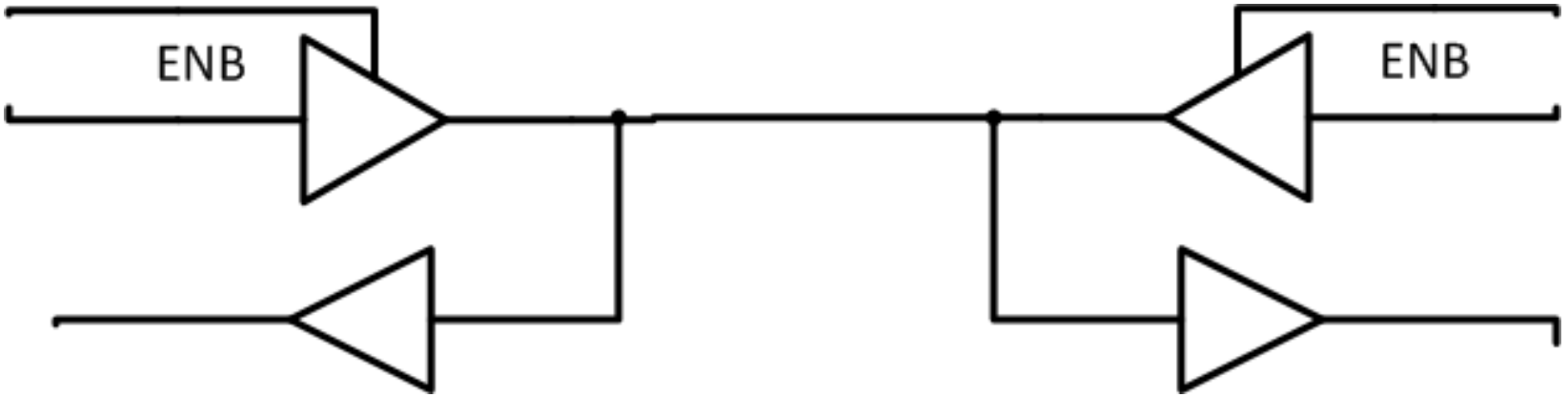


3-State Buffer



A	E	Q
0	1	0
1	1	1
0	0	Z
1	0	Z

Uses for 3-State Buffers



References

See class notes “Beyond Simple Logic Gates” (page 133)