ECED2200 – Digital Circuits

Adders, Subtractors, ALUs

General Notes

- See updates to these slides: www.newae.com/teaching
- These slides licensed under 'Creative Commons Attribution-ShareAlike 3.0 Unported License'
- These slides are not the complete course – they are extended in-class
- You will find the following references useful, see www.newae.com/teaching for more information/links:
  - The book "Bebop to the Boolean Boogie" which is available to Dalhousie Students
  - Course notes (covers almost everything we will discuss in class)
  - Various websites such as e.g.: www.play-hookey.com
  - The book "Contemporary Logic Design", which was used in previous iterations of the class and you may have already

ADDERS & SUBTRACTORS

Half Adder

$$\begin{array}{r} 1\ 0\ 1\ 0\ 0\ 1 \\ +\ 0\ 1\ 0\ 1\ 1\ 0 \\ \hline \end{array}$$

Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half Adder - Sum

A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

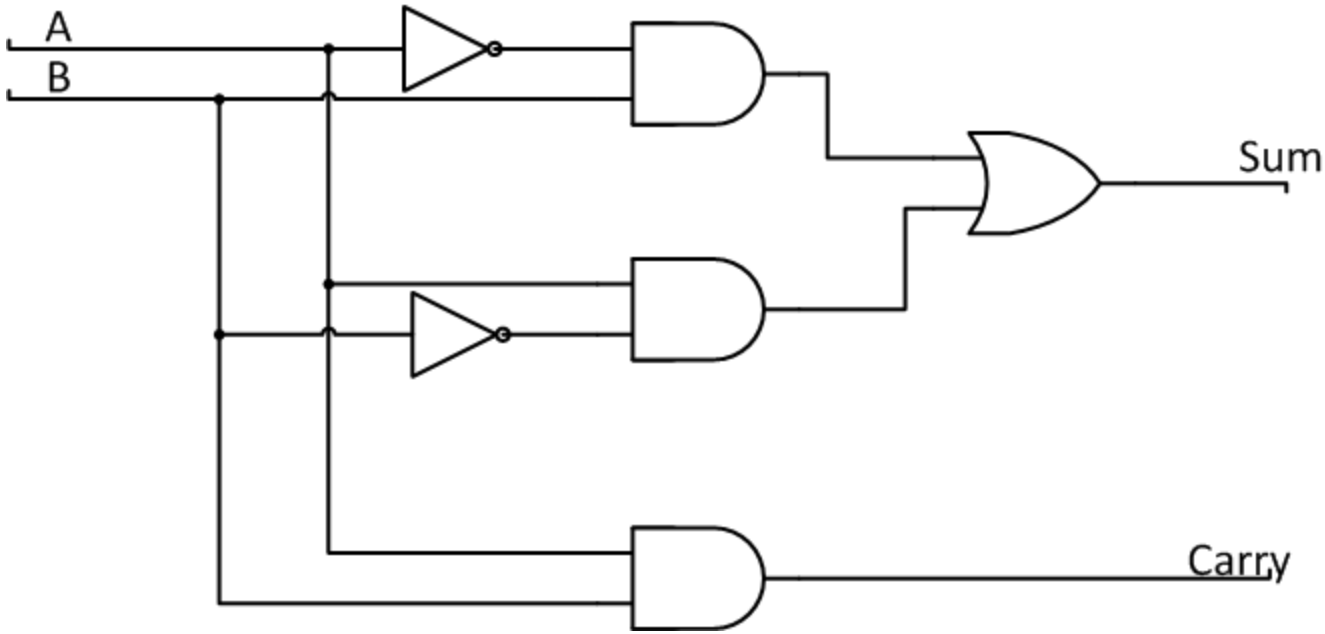
$$S = m_1 + m_2 = \overline{A} \bullet B + A \bullet \overline{B}$$

Half Adder - Carry

A	B	Carry
0	0	0
0	1	0
1	0	0
1	1	1

$$C = m_3 = A \bullet B$$

Half Adder - Circuit



Half Adder – Can we Improve it?

$$S=\overline{A}\bullet B+A\bullet\overline{B}$$

No.	Identity	Comments
1	$A+0=A$	Operations with 0 and 1
2	$A+1=1$	Operations with 0 and 1
3	$A+A=A$	Idempotent
4	$A+\overline{A}=1$	Complements
5	$A\bullet 0=0$	Operations with 0 and 1
6	$A\bullet 1=A$	Operations with 0 and 1
7	$A\bullet A=A$	Idempotent
8	$A\bullet\overline{A}=0$	Complements
9	$\overline{\overline{A}}=A$	
10	$A+B=B+A$	Commutative
11	$A\bullet B=B\bullet A$	Commutative
12	$A+(B+C)=(A+B)+C=A+B+C$	Associative
13	$A\bullet(B\bullet C)=(A\bullet B)\bullet C=A\bullet B\bullet C$	Associative
14	$A\bullet(B+C)=(A\bullet B)+(A\bullet C)$	Distributive
15	$A+(B\bullet C)=(A+B)\bullet(A+C)$	Distributive
16	$A+(A\bullet B)=A$	Absorption
17	$A\bullet(A+B)=A$	Absorption
18	$(A\bullet B)+(\overline{A}\bullet C)+(B\bullet C)=(A\bullet B)+(\overline{A}\bullet C)$	Consensus
19	$\overline{A+B+C+\ldots}=\overline{A}\bullet\overline{B}\bullet\overline{C}\ldots$	De Morgan
20	$\overline{A\bullet B\bullet C\bullet\ldots}=\overline{A}+\overline{B}+\overline{C}\ldots$	De Morgan
21	$(A+\overline{B})\bullet B=A\bullet B$	Simplification
22	$(A\bullet\overline{B})+B=A+B$	Simplification

Half Adder – Can we Improve it?

$$S = \overline{A} \bullet B + A \bullet \overline{B}$$

19) $$\overline{C} \bullet \overline{D} = \overline{C + D}$$

$$= \overline{\overline{A} \bullet B} + \overline{A \bullet \overline{B}}$$

$$= \overline{\overline{A} + \overline{B}} + \overline{\overline{A} + B}$$

20) $$\overline{C} + \overline{D} = \overline{C \bullet D}$$

$$= \overline{A + \overline{B} \bullet \overline{A} + B}$$

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22	$(A \bullet \overline{B})+B=A+B$	Simplification

Half Adder – Can we Improve it?

$$= \overline{A+\overline{B} \bullet \overline{A}+B}$$

$$= \overline{\left(A \bullet \overline{A}\right)+\left(A \bullet B\right)+\left(\overline{A} \bullet \overline{B}\right)+\left(B \bullet \overline{B}\right)}$$

$$= \overline{(0)+\left(A \bullet B\right)+\left(\overline{A} \bullet \overline{B}\right)+(0)}$$

$$= \overline{\left(A \bullet B\right)+\left(\overline{A} \bullet \overline{B}\right)}$$

19) $\overline{C} \bullet \overline{D} = \overline{C+D}$

$$= \overline{\left(\overline{\overline{A}+\overline{B}}\right)+\left(\overline{A+B}\right)}$$

No.	Identity	Comments
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Half Adder – Can we Improve it?

$$= \overline{\left(\overline{\overline{A}+\overline{B}}\right)+\left(\overline{A+B}\right)}$$

20) $\overline{C}+\overline{D}=\overline{C \bullet D}$

$$= \overline{\left(\overline{A}+\overline{B}\right)\bullet\left(A+B\right)}$$

$$= \left(\overline{A}+\overline{B}\right)\bullet\left(A+B\right)$$

20) $\overline{C}+\overline{D}=\overline{C \bullet D}$

$$= \left(\overline{A \bullet B}\right)\bullet\left(A+B\right)$$

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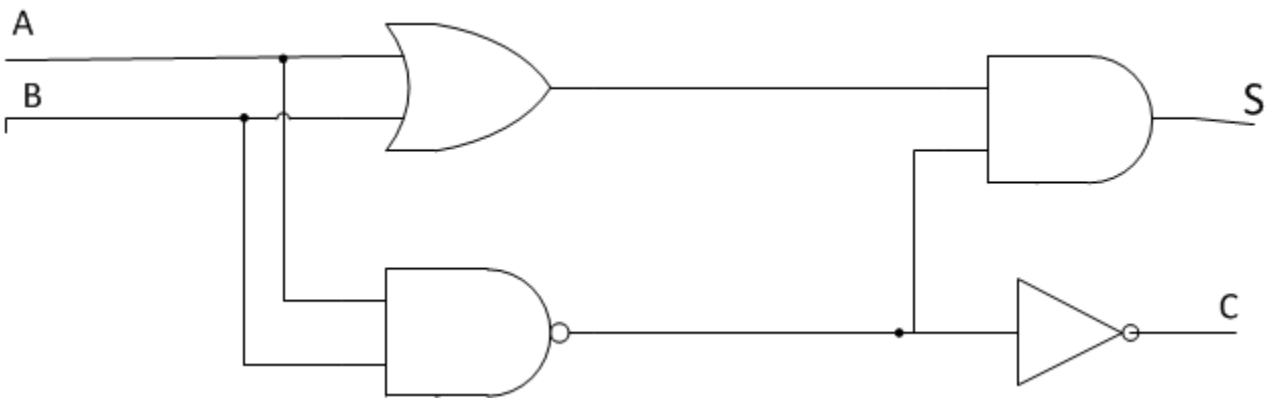
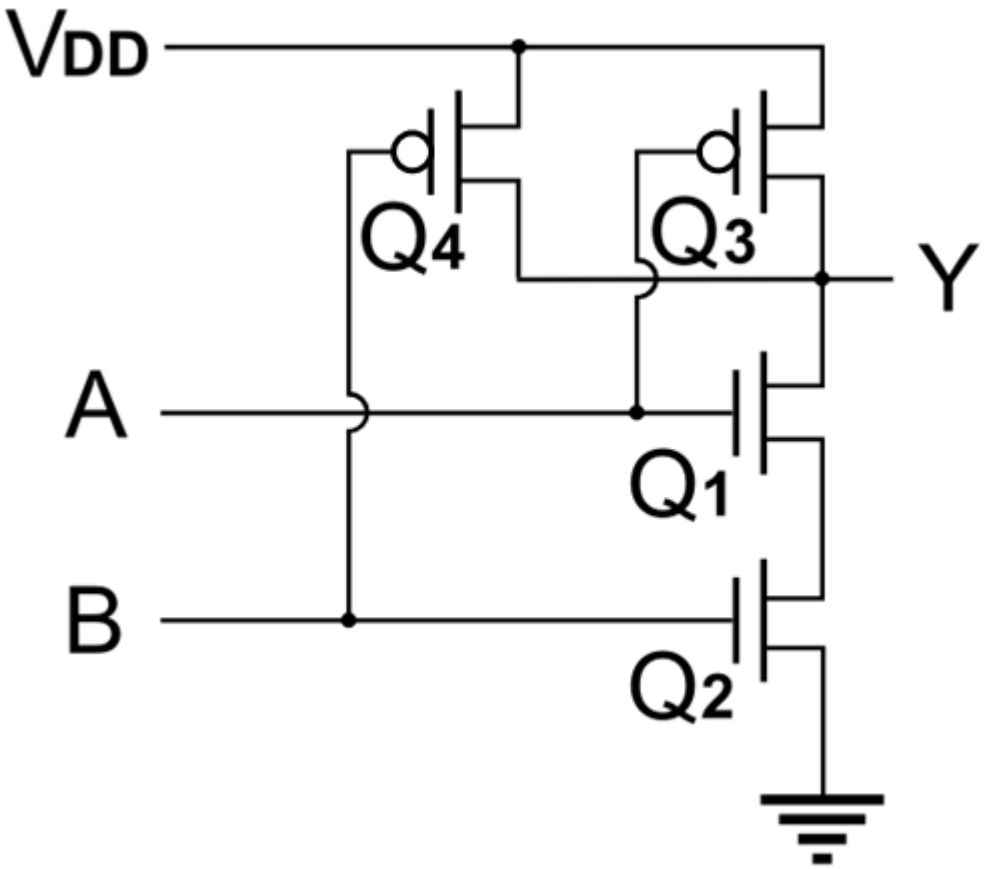
21	$(A+\overline{B}) \bullet B=A \bullet B$	Simplification
22	$(A \bullet \overline{B})+B=A+B$	Simplification

Half Adder – Improved Implementation



NAND Gate Implementation



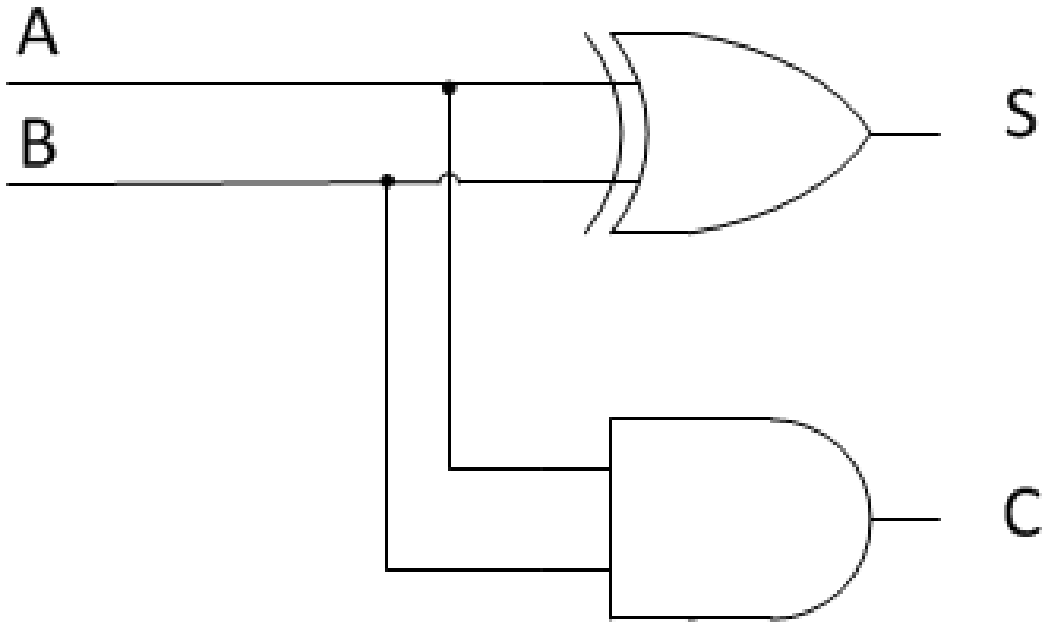
Source: http://commons.wikimedia.org/wiki/File:NAND_gate_(CMOS_circuit).PNG

Half Adder – Easier Sum

A	B	Sum
0	0	0
0	1	1
1	0	1
1	1	0

$$S = A \oplus B$$

Half Adder – Classic Implementation



Full Adder

Ci

1 0 1 0 0 1 A

+ 0 1 0 1 1 0 B

S

Co

Full Adder

A	B	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Adder – Sum Out

A	B	Carry In	Sum
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

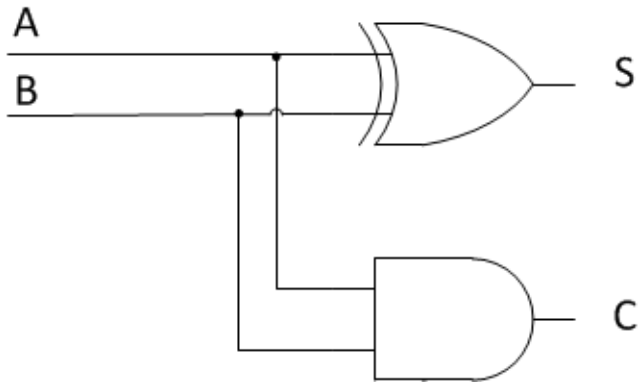
$$S = m_1 + m_2 + m_4 + m_7$$

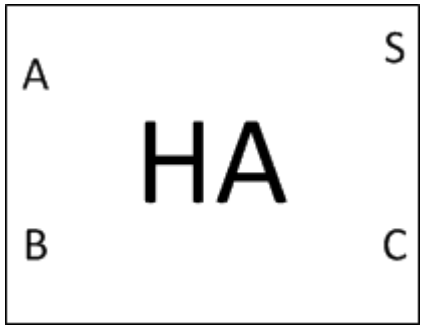
Full Adder – Carry Out

A	B	Carry In	Carry Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

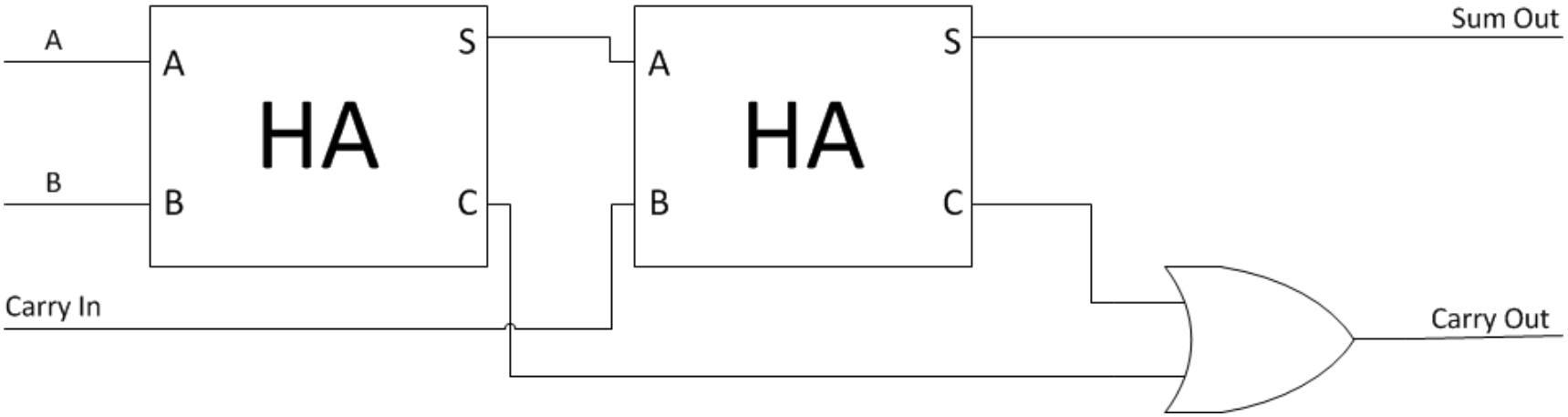
$$Co = m_3 + m_5 + m_6 + m_7$$

Full Adder Built from Half Adders



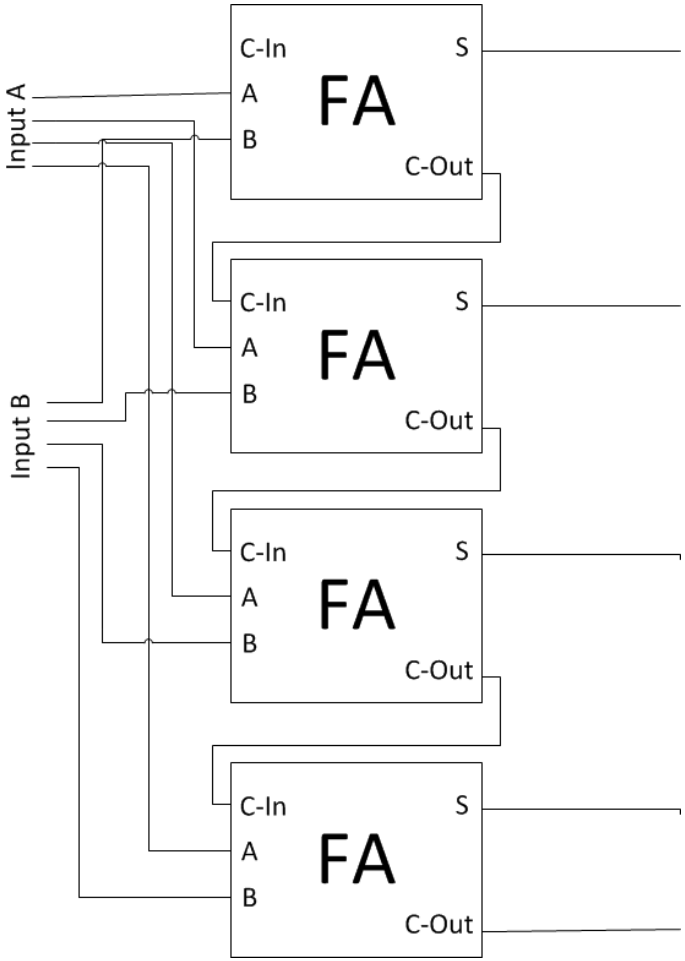


Full Adder Built from Half Adders

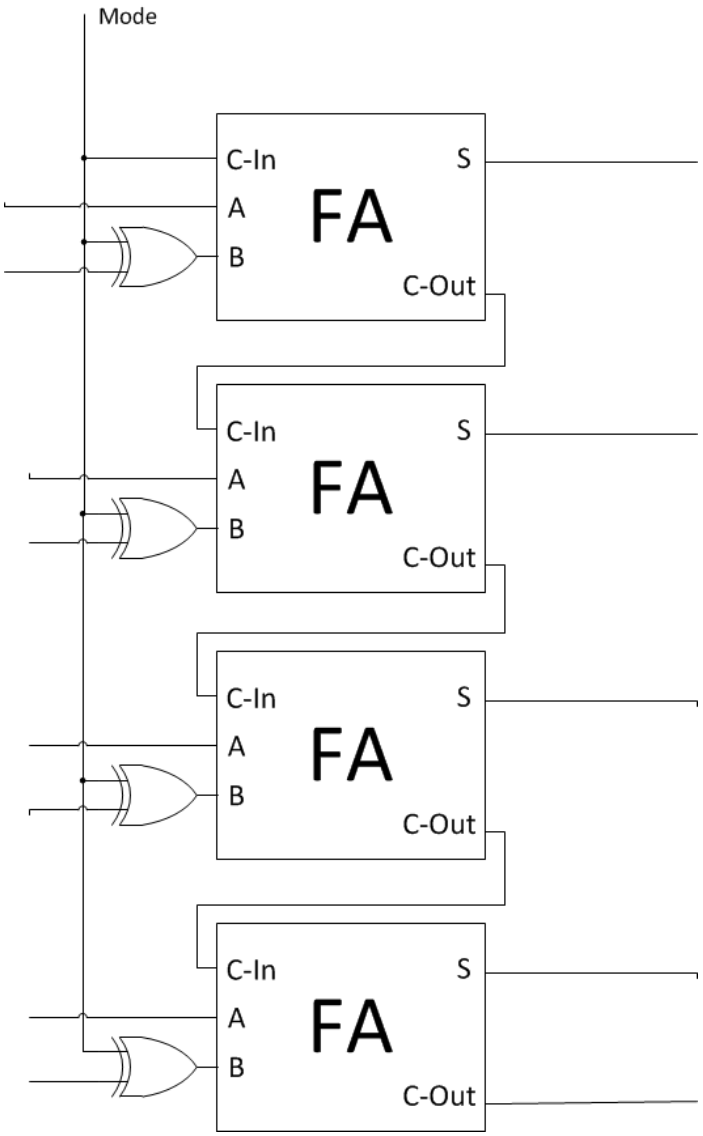


A	B	Carry In	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

N-bit Adders



Subtractors



Arithmetic Logic Unit (ALU)

Arithmetic Logic Unit (ALU)

Section Summary

- See ECED Notes “Arithmetic Logic Units” (ALU) Page 64/65/66